Blue ICE

A 100 Watt Power Amplifier

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1. Table of Contents

1. Table of Contents	ii
2. Introduction	1
3. Topology	1
4. Output stage	
5. Voltage Amplifier	
6. Input Stage	
7. Thermal and Mechanical Issues	
8. Blue ICE Schematic	
9 References	

2. Introduction

In this document a design for an 'audiophile' power amplifier capable of 100 Watts average power dissipation into 8 Ω is presented. Relevant theory is briefly discussed. Testing is conducted using suitable equipment. Where such equipment is unavailable a simulator will be used to find a plausible result. In the case of total harmonic distortion, a reputable SPICE simulator produces 0.006% THD for 1 kHz at 50 Watts into 16 Ω resistive. There are other factors which the simulator does not account for, so this could be considered a theoretical minimum. In any case it is well below the minimum distortion that can be heard (by any set of ears) in a sinusoid (around 0.1%). The distortion is specified in this way because the amplifier will be primarily used with a 16 Ω loudspeaker cabinet.

3. Topology

H C Lin presented the three stage transistor power amplifier topology in 1956. It has been widely accepted by consumers, audiophiles and industry alike. This amplifier is based on his topology and this document is split into four main sections. The output stage (perhaps a more helpful name would be "the current amplifying stage" as this is descriptive), the voltage amplifier stage and the input stage. Design begins at the output.

Below is a standard topology without values to give a general idea of what a power amp circuit design looks like.

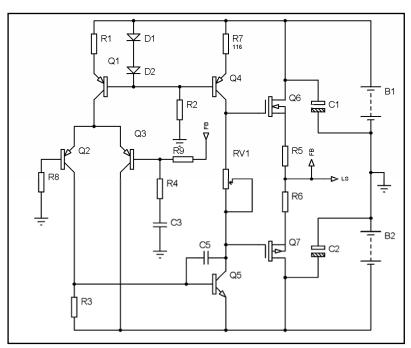


Figure 1: General Simple Power Amplifier

The output stage is composed of Q6, Q7, R5 and R6. The voltage amplifier Stage (hereafter VA) is Q5 which is fed by the constant current source (CCS) consisting of Q4, R7, D1, D2 & R2 (the diodes and R2 are shared with the Input stage CCS). RV1 biases the output stage to the edge of conduction.

The input stage is the differential pair Q2 & Q3 fed by the CCS of Q1 and R1. R3 drops the V_{BE} of Q5. No voltage is swung here as the VA is current driven. The capacitor C5 is the compensation capacitor. Its value is difficult to find manually. A simulator is always used. Even then the value is subject to 'adjust on test'. As frequency increases C5 looks lower impedance and current is fed back from the collector of Q5 to the base, reducing the gain. Phase shifts introduced by time constants either due to device capacitances or real capacitances conspire to produce more than 180° of phase shift at the output (w.r.t the input). Because feedback is taken from the output to the input (by means of the differential pair) the gain must be less than unity when the phase shift reaches 180°. If this is not achieved the feedback will be positive and the amplifier will be an oscillator!

4. Output stage

The output stage (OPS) in the case of this amplifier is an Emitter Follower (EF), Bipolar Junction Transistor (BJT) type. Looking at the final circuit diagram (Figure 3) the output stage is formed by two parallel output pairs Q12, Q13, Q14 Q15. Because these are power BJTs, h_{fe} is low typically a minimum of 15[1]. This requires a driver stage to avoid loading the VA Stage. Q10 and Q11 are the drivers. R13, R14, R15, R17, R18, R19, R20, R21, Q16, Q17 D3 & D4 form a protection circuit that will avoid destruction of the output devices in the event of too larger current flowing in these devices. Protection will be considered later.

Between the drivers is a 200 Ω resistor in parallel with a 100n capacitor. The drivers are not connected to the output. This appears to be an under appreciated advantage. The more popular arrangement where the drivers each have a resistor from the emitter to the output rail offers inferior (from an efficiency perspective) turn off characteristics. SPICE has been used to show this. A further advantage of this arrangement the capacitor allows the transient signals (such as at turn off and turn on (around the crossover region)) to pass freely between the base regions of the drivers. This is often collected along with the reverse biasing of the device which is being turned off under the term 'charge suckout'. A more complete argument is given in Self [2].

To produce an average power of 100 Watts in 8 Ω 28.28 V_{RMS} is required, this corresponds to 40 V_{pk} and 5 A_{pk} load current. The 5 A is split between two NPN and two PNP devices to avoid destruction of the devices. Each device will carry a 2.5 A_{pk} equal current sharing is ensured by the "emitter resistors" R22 R23 R24 & R5. The maximum base current required to drive the maximum peak load current is 0.33 A_{pk} . This is delivered by the drivers. The drives minimum h_{fe} is 30. In practice it is rarely found to be less than 100. As an aside, if a design were drawn up for a <10 watt power amplifier with a BJT output stage a single pair of MJE340/MJE350 devices would be a good choice. If they are selected for high h_{fe} (h_{fe} max is 240) it would be possible to avoid a driver stage, something which is usually mandatory with a BJT OPS. The VA must deliver a theoretical maximum of 11mA to the drivers but in practice 3.33mA is more likely.

5. Voltage Amplifier

The voltage amplifier (VA) provides all of the voltage gain. It is simply a common emitter amplifier. The DC conditions are controlled by the global feedback loop. In this case a Darlington pair has been used. The Darlington increases the open loop gain. Feedback limits the closed loop gain to 32dBV. The forward gain is the product of the devices h_{fe} s which in this case is in the order of 10000. The feedback factor at maximum output and below the dominant pole frequency is therefore 250. This is two orders of magnitude larger than if a single transistor had been used. If the amplifier locks up the current from ground into Q8 would destroy it. R11 prevents this. Astute readers will realise that R11 is under rated for this task. I would expect it to smoke heavily. Lockup is only likely under testing. When the amplifier goes into service any such problems should have been overcome. So this is not a problem as the operator will quickly remove the power. A current limited supply would circumvent this problem. R12 provides a current path for charge leaving the base of Q9 when it is being switched off.

The constant current source formed by D1 D2 R5 R8 and Q6 supplies 7mA to the VA and biasing network. The diodes drop 0.7 Volts each and the current flows to ground through R5. Q6 is turned on removing one diode drop to its base – emitter junction. This leaves 0.7Volts across the 100 Ω resistors R8, 7mA flows. C12 decouples the voltage reference formed by D1 D2 and R5.

Q9 R30 and RV1 form a voltage reference normally referred to as an amplified diode. Significant improvements are possible over the circuit used here for example [3]. However this circuit is satisfactory. Its operation relies on the current in RV1 and R30 being dependant only on the resistance, because the voltage is constant. The (adjustable via RV1) current flows in R9 and hence the collector - emitter voltage of Q9 is set as is the voltage between the bases of the driver transistors. R30 is used to prevent the total base emitter resistance being set to zero. Q9 is an MJ340 because this can be mounted easily to a heat sink next to the power devices. This provides thermal (negative) feedback and counters thermal runaway; however under heavily over biased conditions the feedback will not be fast enough to save the output stage. In this case the DC protection circuitry will save the OPS instead. This is possible because at some high current the voltage across R23, R18 and R19, in the NPN case, will become enough to turn on Q16 and remove the current drive from Q10. No load is required for the protection circuitry to work. In Figure 3 the values of the protection components are suitable for 16 Ω operation for 8 Ω operation they must be changed to accommodate the higher currents.

6. Input Stage

The input stage is a differential pair or long tailed pair. Its purpose is to compare a reduced version of the output voltage with the input and feed the error signal (i.e the difference) to the VA. To obtain low DC offset an emitter degenerated current mirror is used to keep the current flowing out of the collectors of Q2 and Q3 the same (under DC conditions). The current mirror is made from Q4, Q5, R6 and R7. The degeneration operates on the small signal emitter resistance re' which is approximately the reciprocal of gm. gm is found from the collector current. re' in this case is around 7.2 Ω so the 150 Ω degenerating resistors are easily dominant. Slight variations in re' due to device mismatch are easily swamped by the 150 Ω resistors.

The CCS feeding the differential pair must be able to charge the compensation capacitance C13 quickly enough to avoid slewing in the audio bandwidth. An approximate calculation is $I_{C13} = 2 \times \pi \times f_{MAX} \times C_{13} \times V_{pk}$. For the amplifier in question the result is 2.76mA. To allow some room for manoeuvre it is wise to at least double this amount. When using a current mirror all of the current in the differential pair can be directed to one leg and the other only have a very small current flowing. In the case of a resistively loaded differential pair only one half of the current can be switched. In this case the figure above should be quadrupled. If a current mirror was not used here (and the CCS output was doubled) Q1 would run very hot, reducing its life. When fitting the compensation capacitor it is acceptable to assume 80pF of stray capacitance and use a 470pF capacitor.

There is a band limiting input filter on the front of the amplifier [4]. R2 and R3 must equal the feedback resistance. This avoids generation of even harmonics in the differential pair. C6 R2 R3 and r_{be} form the low pass filter rbe is about 7.7 k Ω at the operating point. The high pass filter is formed by R1 and C5. These limit the bandwidth to the range of human hearing.

7. Thermal and Mechanical Issues

This document indicates that a 100 Watt amplifier is being designed. However, except for the use of parallel output devices, the text so far refers to 50 Watts. Provided the output transistors can withstand the power dissipation and will not get too hot. The limit on developed load power is the resistance of the load. The output devices have been addressed already. The thermal design is considered here.

7.1. Thermal Issues

Using the datasheet for the TIP3055 and assuming that the ambient temperature is 25°C a thermal diagram can be drawn. From [1] the Junction to Case thermal resistance is 1.4°CW⁻¹. The thermal pads that have been used are rated at 0.45°CW⁻¹. The worst case power dissipation is for a sinusoidal input voltage. The power dissipated in a fictional NPN device which represents the two real NPN devices is given by [5]

$$P_{MAX} = \frac{V_S^2}{\pi^2 \cdot R_I}$$

V_s is the supply voltage (50 Volts)

V_p is the peak output voltage

R_L is the load resistance

Solving for the amplifier under discussion ($R_L = 8\Omega$) $P_{MAX} = 31.66$ Watts for one cycle. This value should be doubled because all devices (NPN and PNP) will be mounted on the same heat sink. The NPN devices dissipate 31.66 Watts averaged *over one cycle* and the PNP devices do the same in the other, consequently the average dissipation is 63.32 watts.

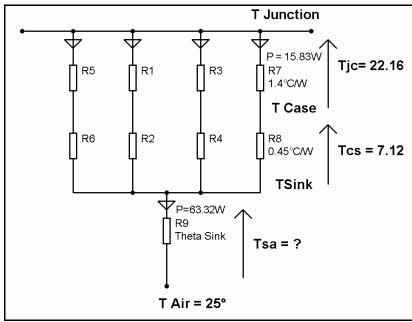


Figure 2: Thermal Diagram

In the above diagram power takes the place of current, temperature is analogous to voltage and thermal resistance is represented by electrical resistance. To find the minimum value of heatsink thermal resistance the maximum temperature rise across the resistance must be decided. The datasheets [1] [6] give T_{Jmax} as 150°C. Let the value of junction temperature that must not be exceeded equal 100°C. Then the value of T_{sink} = 70.72°C.

$$\theta_{\sin k} = \frac{T_{\sin k} - T_{air}}{P_{\sin k}}$$

$$\theta_{\sin k} = \frac{70.72 - 25.00}{63.32}$$

$$\theta_{\sin k} = 0.722^{\circ}CW^{-1}$$

This is the minimum value of heatsink to satisfy the requirement. A value of 0.64°CW⁻¹ was used to give some room for quiescent dissipation.

7.2. Mechanical Considerations

If you are not familiar with heat sinking then you should read the relevant sections of the "Ice 'n' Lemon" Project on the ICE amplifiers website. The example test procedure in "Ice n Lemon" can be adapted for this amplifier also.

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Blue ICE Schematic

8. Blue ICE Schematic

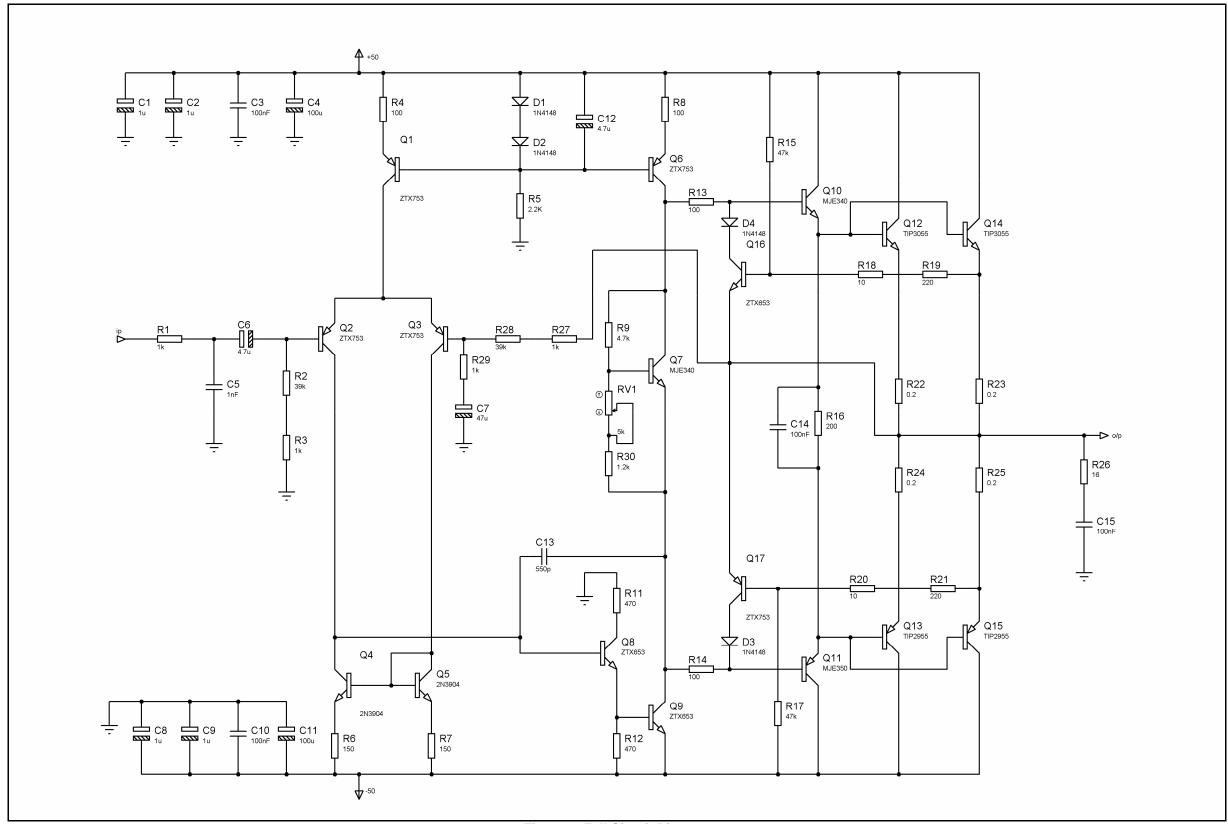


Figure 3: Full Circuit Diagram

9. References

[1] "TIP3055 Datasheet", ST Microelectronics, 1999

[2] Self, D "Audio Power Amplifier Design Handbook", Third Edition, Newnes, 2003 pg 114

[3] Hawksford M J, "Optimization of the Amplified-Diode Bias Circuit for Audio Amplifiers" J. Audio Eng. Soc. Volume 32 Number 1/2 pp. 31-33; January/February 1984

[4] Green J E "First order filter design for power bandwidth limiting", 2006 http://www.iceamplifiers.co.uk

[5] Green, J E "Power Dissipation in Semiconductor Devices Using Calculus", 2005 http://www.iceamplifiers.co.uk

[6] "MJE340 Datasheet", Fairchild Semiconductor, 2001