EEE225: Analogue and Digital Electronics

Lecture V

James E. Green

Department of Electronic Engineering
University of Sheffield
j.e.green@sheffield.ac.uk

This Lecture

Differential Stage Problems

Problems with the input (differential) stage

1. Half of the differential signal is wasted. The collector of T_2 is connected to the negative supply. The output from the differential stage is ΔI for a given ΔV input (see lecture 3 slide 5) but we can do better...
2. The balance of collector current in T_1 and T_2 is difficult to maintain due to loading effect of T_3 - this leads to DC offset at the output.
3. The current flowing into the base of T_1 and T_2 is quite high. This input current has to be supplied by the signal source. The basic opamp has a low input resistance compared to a commercial opamp.
4. The effective load resistance of the differential stage (approximately // combination of R_1 and r_{be3}) is very low so the differential stage has low gain.

VAS and OPS Problems

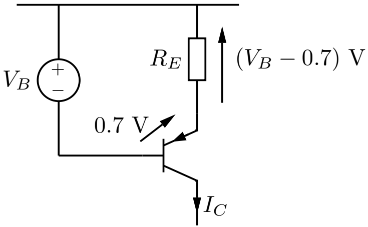
Problems with the voltage amplification stage

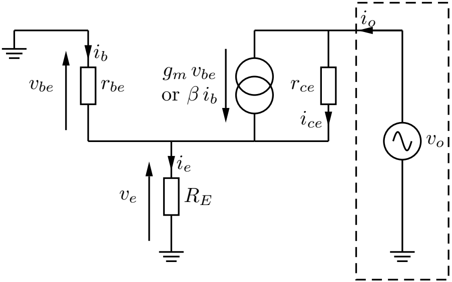
1. R_{VA} needs to be quite small to maintain correct DC (quiescent) conditions – the quiescent current of T_3 flows through R_{VA} – but the gain of the VAS is proportional to R_{VA} so a very large value is desirable which the DC current does not permit.

Problems with the output stage

1. The input resistance of T_4 and T_5 depends on the external opamp load resistance, this affects the effective load resistance of the VAS altering its gain.
2. The output resistance of the emitter follower is dependent on the source resistance driving it.
3. Without OPS biasing T_4 and T_5 will give rise to severe crossover distortion (as per Amplifier Lab).

From lecture 3, the resistance looking out of T_3's collector is $\approx R_{VA}$. Increasing the value of R_{VA} is desirable as it increases gain. However T_3's quiescent collector current has to flow through R_{VA} limiting its value. R_{VA} can be replaced by a current source (left) and its small signal model (right).





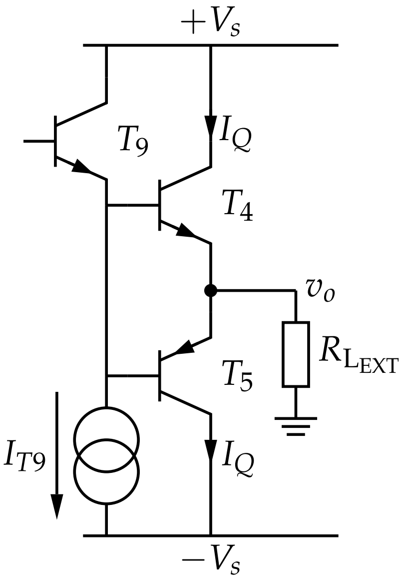
The effective resistance looking into the current source output – it's output resistance – will become the new R_{VA}. For analysis see handout "Small Signal Output Resistance of a Simple Current Source". In brief $r_o \approx r_{ce}\,(1+\beta)$.

The output stage's input resistance (looking into T_4 and T_5) is affected by the external load resistance $R_{L_{\mathrm{EXT}}}$. The VAS gain is affected as R_{VA} is now not so low as to be dominant. T_9 can be added to partially overcome this loading effect. T_9 forms a Darlington pair with whichever of T_4 or T_5 is conducting. The input resistance of T_4 is

$$r_{i4} = r_{be4} + (\beta_4 + 1)\ R_{L_{\mathrm{EXT}}} \quad (1)$$

The input resistance of T_9 is,

$$r_{i9} = r_{be9} + (\beta_9 + 1)\ r_{i4} \quad (2)$$

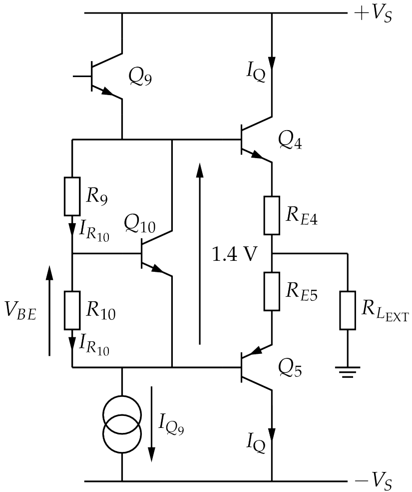


The now higher resistance looking towards T_3's collector acts to increase the output resistance of the amplifier as well. The output resistance of an emitter follower is

$$r_o = \frac{r_{be}}{\beta} + \frac{R_S}{\beta} \tag{3}$$

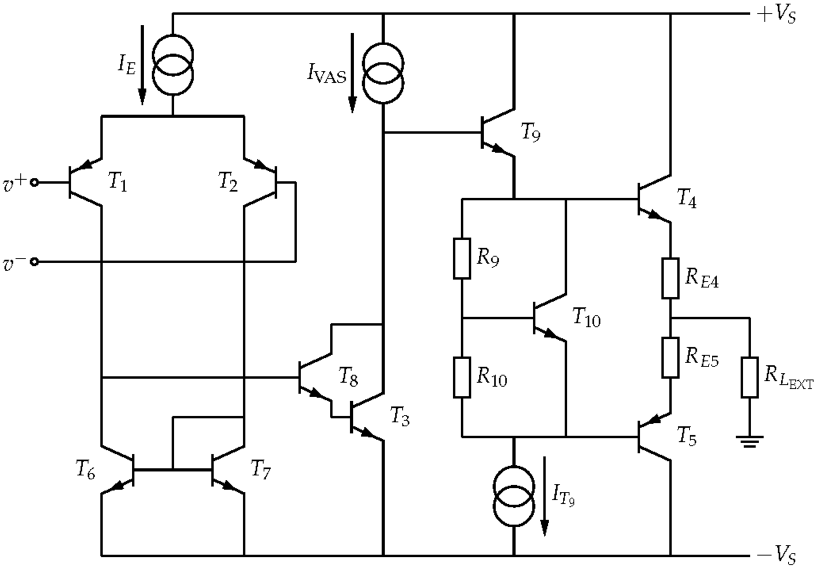
Without T_9 the R_S for T_4 is the collector load resistance of T_3 which has been made very large to maximise the VAS gain. This increases the OPS output resistance. Including T_9 allows the input resistance of the OPS (T_9, T_4 and T_5) to be large and the output resistance of the OPS to be small.

These two problems (firstly the low input resistance of the OPS, and secondly, having increased the source resistance driving the OPS, the OPS output resistance increases) unveil the true nature of the transistor – an imperfect impedance transformer. The ideal OPS would present infinite input resistance to its source and present zero output resistance to its load. Adding T_9 improves the resistance transforming property.



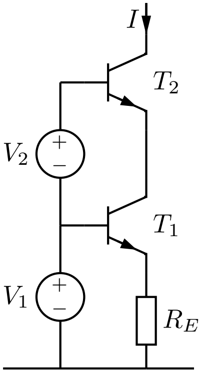
T_4 and T_5 don't conduct until $|V_{BE}| > 0.7\ V$.

When the bases of T_4 and T_5 are connected together there is a region in which the signal is permanently lost. A circuit to spread the bases by approximately 2 V_{BE} is inserted between them. This is sometimes called an amplified diode. The V_{BE} of T_{10} appears across R_{10} causing a current $I_{R_{10}}$. Assume $I_{B_{(T_{10})}} = 0$ so $I_{R_{10}}$ must flow in R_9 also. Reducing R_{10} increases the current through it (voltage is very nearly fixed). The voltage across R_9 must increase... $I_{R_{10}}$ should be a fraction of I_{T_9}.

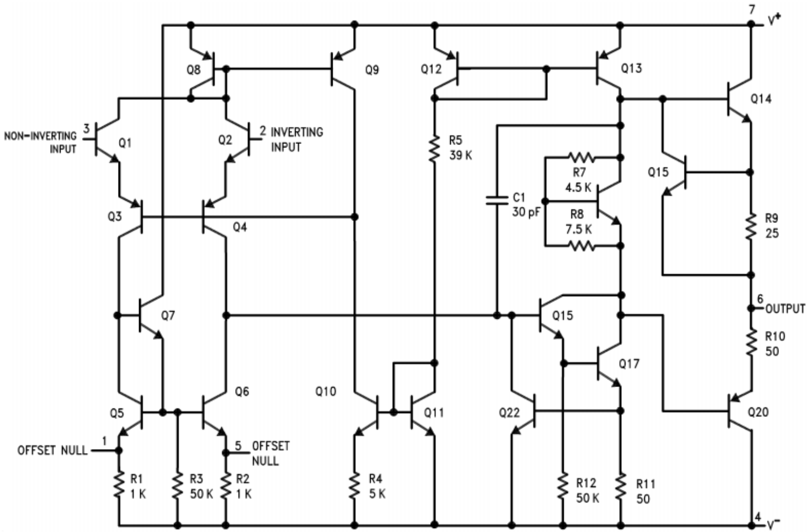

$+V_S$
I_E
I_{VAS}
T_9
v^+
T_1
T_2
T_4
v^-
R_9
R_{E4}
T_{10}
R_{E5}
$R_{L_{EXT}}$
T_8
R_{10}
T_3
T_5
T_6
T_7
I_{T_9}
$-V_S$

- I_E, I_{VAS} and I_{T_9} set up the DC or quiescent conditions by defining currents.
- Current sources are normally current mirror circuits with one or two additional components to set the DC conditions. The simple current source tends not to see much use.
- The current mirrors can be connected together to allow the ratio of supplied currents to be set. The simple current source has no similar advantage.
- I_E is typically $10 - 50\ \mu\mathrm{A}$. I_{VAS} is typically $100 - 200\ \mu\mathrm{A}$ and I_{T_9} is typically $1 - 5\ \mathrm{mA}$
- This improved circuit reduces all of the problems. However it is one possible implementation of a simple opamp. Real opamps tend to be somewhat more complicated.
- Notice the general lack of resistors - transistors are easy to produce in ICs, resistors (especially precise values) are difficult and expensive. Designers will always use one or more transistors if possible.

- A common emitter amplifier (T_1) connected to the input of a common base amplifier (T_2).
- Prevents voltage swing on the collector of (T_1) by making the resistance looking into T_2's emitter small.



- Enhances the bandwidth of the CE stage by reducing the "Miller effect".
- Depletion capacitance of T_1's reverse biased CB junction couples signal voltages from the collector to the base developing undesirable negative feedback effect – overcome by preventing significant voltage swing on this node.
- The voltage swing on T_2's collector is OK because T_2's base is a fixed voltage - it does not have the input signal on it and is a low resistance path to ground for signals.


7
V+
Q8
Q9
Q12
Q13
Q14
NON-INVERTING INPUT
3
Q1
Q2
2 INVERTING INPUT
R5
39 K
C1
30 pF
R7
4.5 K
R8
7.5 K
Q15
R9
25
Q3
Q4
Q7
6
OUTPUT
Q15
R10
50
Q17
Q6
Q10
Q5
Q11
Q22
Q20
OFFSET NULL
1
5
OFFSET NULL
R1
1 K
R3
50 K
R2
1 K
R4
5 K
R12
50 K
R11
50
4
V−

Review

- Introduced a one transistor current source
- Re-iterated concept of transistor as an active component for transforming resistances (a transfer-resistor) by looking at the OPS input and output impedances
- Introduced the amplified diode, and cascode circuit
- Briefly discussed a simplified schematic of a real opamp (circa 1968).

The key points about these integrated circuit building blocks are,

1. To understand the bigger circuits one must first be confident with all their various circuit blocks.
2. To put the circuit blocks together one must appreciate how they are likely to interact.
3. Reducing the problem to the components which are dominant is one key to an easy analogue life...
4. ...the other is practice, and reading!