Op-Amp Anatomy

Basic op-amp circuit

Introduction

Figure 1 shows a circuit that contains the basic elements of an op-amp. The elements are the simplest circuits that will perform the required basic function and so are not optimised to give

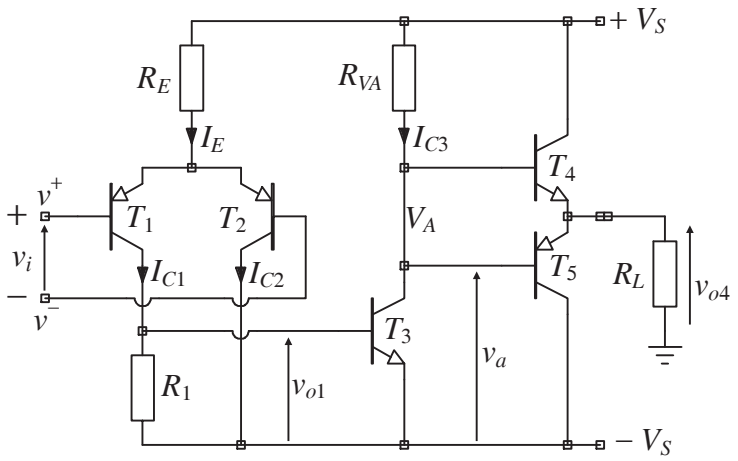

Figure 1

a good op-amp performance. The treatment that follows looks first at this basic circuit from a dc condition point of view and then explores the way the circuit responds to signals which can be regarded as small changes superimposed on the dc conditions. The study of the response of the circuit to small changes in dc conditions is called "small-signal" (ss) analysis. In principle ss analysis yields results that are frequency dependent but here we assume that frequencies are sufficiently low that no reactive effects are significant.

After identifying the problems associated with the basic circuit of figure 1, refinements are added to the circuit that increase complexity but also make the design perform more effectively as an op-amp.

Evaluating dc conditions

There are some key ideas about op-amps that must be bourne in mind when working out dc conditions:

- No op-amp will work properly without feedback. The feedback controls the gain of the circuit but also performs a crucial role in defining the circuit dc conditions. The feedback will alter the dc value of v_i in order to achieve the internal voltage drops required for proper operation. This means that if $v_o = 0$, v_i will be at the value it needs to have in order to make $v_o = 0$ and in a good op-amp this value will be very small.
- The "differential input voltage", v_i in figure 1, is the difference $v^+ - v^-$.

- The "common mode input voltage" is the average of v^+ and v^-, ie, $(v^+ + v^-)/2$

In the circuit of figure 1 the common mode input voltage will affect the internal amplifier currents so the assumption will be made here that $v^+ \approx v^- \approx 0$. It is not difficult to apply the process below to a case where common mode voltage is non-zero. Whatever the common mode voltage, $v^+ \approx v^-$ will be a valid assumption.

If $v^+ \approx v^- \approx 0$, V_{E1} and $V_{E2} \approx 0.7$ so $I_E \approx (V_S - 0.7)/R_E$. I_E splits between T_1 and T_2 to form I_{C1} and I_{C2}. I_{C1} has two functions; it must create a voltage drop of 0.7 V across R_1 in order to bias T_3 into conduction and it must provide the necessary base current for T_3. This means that I_{C1} will be $0.7/R_1 + I_{C3}/h_{FE3}$. The value of I_{C3} varies with V_A and hence with V_O but assuming $V_A = 0$, $I_{C3} = V_S/R_{VA}$. I_{C2} is returned directly to the negative supply. In the case where $v^+ \approx v^- \neq 0$, there is a common mode input voltage, v_{cm}, and $I_E \approx (V_S - v_{cm})/R_E$. The rest of the process is as just described.

The biggest problem with this simple circuit is that a small value of I_E is desirable to give the op-amp a high input resistance and for keeping noise to a minimum. It is desirable to have an equal split of I_E between I_{C1} and I_{C2} in order to minimise input stage imbalance which causes offset problems. I_{C1} supplies both I_{b3} and I_{R1} and although I_{R1} is reasonably predictable, I_{b3} depends upon h_{FE3} which may vary from one op-amp to another. This variation can lead to relatively large imbalances between I_{C1} and I_{C2}. A remedy for this problem will be described later in the "refinements" section.

Evaluating signal related behaviour

The behaviour of the circuit towards signals is evaluated with the help of ss models of the circuit. Since even the simple circuit of figure 1 contains several transistors it is most useful to look at the behaviour of each stage in turn. The objective of the analysis is to identify which circuit components are important players in key performance factors such as voltage gain. We will start the consideration of signal related effects by reviewing the ss behaviour of standard transistor connections.

Small signal review

The common emitter (CE) connection

The common emitter connection is a connection that gives a large voltage gain. It can be configured using either n-p-n or p-n-p transistors as shown in figure 2. Both the n-p-n and p-n-p versions have the same small signal equivalent circuit shown in figure 3. The resistors R_S are the Thevenin equivalent resistance feeding the base and it is assumed that the bias circuit is included within R_S. R_L represents the total resistance between the collector node and signal ground - it is often called the "collector load resistance".

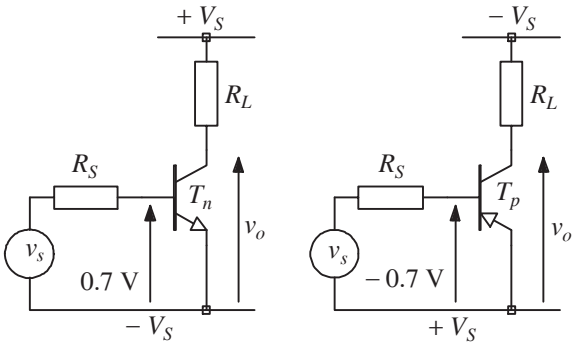

Figure 2

An n-p-n (left) and a p-n-p (right) common emitter circuit. Note the difference in power supply polarity in the two cases.

The small signal circuit of a CE amplifier is shown in figure 3. R_L usually con-

sists of three parallel components; the collector load required locally for biassing, the effective collector-emitter resistance, r_{ce}, of the transistor and the input resistance of the external load that is being driven by the amplifier. r_{ce} is often sufficiently large to make a negligible difference to this parallel combination and under such circumstances it can be ignored.

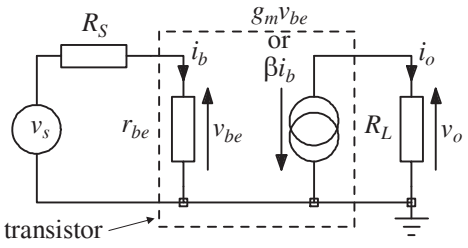

Figure 3

The small signal representation of both the circuits in figure 2

The absence of feedback in the circuit makes it straightforward to find the circuit gain.

At the output, $v_o = i_o R_L = -g_m v_{be} R_L$ since $i_o = -g_m v_{be}$ **(1)**

At the input, $v_{be} = v_s \dfrac{r_{be}}{R_S + r_{be}}$ **(2)**

using **(2)** to substite for v_{be} in **(1)** gives $\dfrac{v_o}{v_s} = -g_m R_L \dfrac{r_{be}}{R_S + r_{be}}$ **(3)**

The important conclusions are

- the gain is inverting (the "–" sign tells us this).
- gain is proportional to g_m (so large g_ms are attractive).
- gain is proprtional to R_L (so large R_Ls are attractive).
- $r_{be} \gg R_S$ must be satisfied to avoid significant input circuit attenuation.

The other parameter of interest for this transistor connection is its input resistance, r_i, looking into the transistor base terminal - that is, the effective resistance between the base terminal and ground. A quick glance at figure 3 will reveal that

$r_i = r_{be}$. **(4)**

The common emitter connection with emitter degeneration

Sometimes CE circuits have a small value of resistance - typically 10s of Ω to low kΩ - between the emitter terminal and ground as shown in figure 4. This resistance is called an "emitter degeneration" resistance. The effect that emitter degeneration has on the shape of the small signal equivalent circuit is simply to add a resistor R_E between the emitter node and ground as shown in figure 5. Unfortunately this addition significantly complicates the small signal analysis, especially if r_{ce} is included in the analisis, because R_E couples the output circuit to the input circuit. In the analysis that follows we will assume that r_{ce} has a negligible effect.

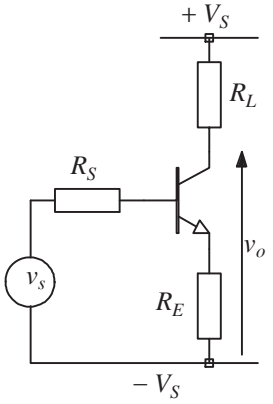

Figure 4

A common emitter amplifier with emitter degeneration

Summing currents at the emitter node in figure 5

$$i_b + g_m v_{be} = i_e \text{ or } \frac{v_{be}}{r_{be}} + g_m v_{be} = \frac{v_e}{R_E} \qquad \textbf{(5)}$$

we need to express v_e in terms of v_s, v_o, v_{be} and the circuit components. Rearranging **(5)** gives

$$v_e = v_{be} R_E \left(\frac{1}{r_{be}} + g_m \right) \approx v_{be} R_E g_m \qquad \textbf{(6)}$$

the simplification is justified since $1/r_{be} = g_m/\beta$ and $\beta \gg 1$

A second equation can be obtained by summing voltages around the input loop

$$v_s = i_b R_S + v_{be} + v_e$$

Recognising that $i_b = v_{be}/r_{be}$ and using **(6)** for v_e this becomes

$$v_s = v_{be} \left(1 + \frac{R_S}{r_{be}} + g_m R_E \right) \qquad \textbf{(7)}$$

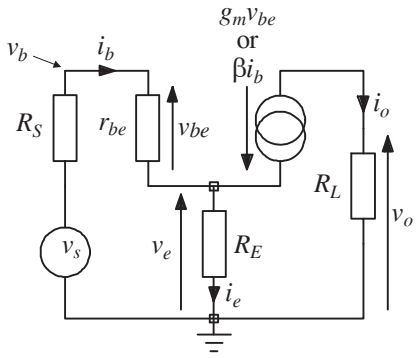

Figure 5
CE circuit with emitter degeneration

At the output side of the circuit, $v_o = i_o R_L$ and $i_o = -g_m v_{be}$. Thus, using **(7)**

$$v_o = -g_m R_L v_{be} = -\frac{g_m R_L v_s}{\left(1 + \frac{R_S}{r_{be}} + g_m R_E \right)}$$

and $$\frac{v_o}{v_s} = -\frac{g_m R_L}{\left(1 + \frac{R_S}{r_{be}} + g_m R_E \right)} = -\frac{R_L}{\left(r_e + \frac{R_S}{\beta} + R_E \right)} \quad \text{where } r_e = 1/g_m \,. \qquad \textbf{(8)}$$

The important conclusions are

- the gain is inverting
- the gain is proportional to R_L
- R_E reduces the gain
- If $R_E \gg 1/g_m$ and R_S/β, gain $\approx -R_L/R_E$

[Note that although R_E is quite commonly found in low frequency amplifiers, for high frequency (10s MHz or higher) amplifier circuits, R_E is almost always undersirable. Indeed one of the big design challenges in RF circuit design is to ensure a low impedance connection between signal ground and transistor emitter. Any impedance in the R_E position interacts with the frequency dependent aspects of the transistor's equivalent circuit in such a way as to encourage instability in the amplifier. Instability in this context means a tendency to oscillate - ie produce an output with no input - at a high frequency, always an undesirable characteristic in an amplifier.]

The presence of R_E also affects the input resistance of the circuit looking into the transistor base terminal. The input resistance is defined by v_b/i_b where v_b is the signal voltage at the base terminal with respect to signal ground.

Summing voltages and using the unsimplified form of **(6)** to express v_e in terms of v_{be}

$$v_b = v_{be} + v_e = v_{be} + v_{be} R_E \left(\frac{1}{r_{be}} + g_m \right) = v_{be} \left(1 + R_E \left(\frac{1}{r_{be}} + g_m \right) \right)$$

and since $v_{be} = i_b r_{be}$ and $g_m r_{be} = \beta$, the input resistance can be written

$$r_i = \frac{v_b}{i_b} = r_{be} + (\beta + 1) R_E \qquad \textbf{(9)}$$

- The input resistance has been increased by an amount $(1+\beta)R_E$ compared to the non R_E case of **(4)**. If $\beta = 300$, say, a typical value for an amplifier transistor, a small R_E can have a significant effect on input resistance.

The "common collector" or "emitter follower" connection

The common collector circuit is one of a class of circuits known as voltage follower circuits. The name arises because the output voltage follows closely the input voltage; the gain is very close to but always less than unity. The common collector circuit can be realised using n-p-n or p-n-p transistors; the n-p-n version is shown in figure 6. As with figures 2 and 4, it is assumed that the effective bias circuit resistance is included in R_S. Notice the similarity to the common emitter with emitter degeneration circuit of figure 4 - the only difference between that and figure 6 is that in figure 6 there is no R_L and the output is taken across R_E.

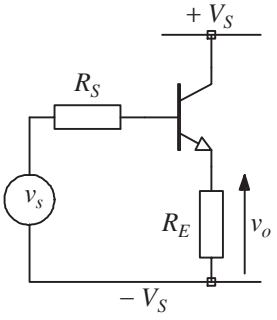

Figure 6

The emitter follower circuit

The small signal equivalent circuit of the emitter follower is shown in figure 7 which has similarities with figure 5. The analysis is very similar to that associated with figure 5 except that v_e has become v_o and does not now need to be eliminated. The analysis begins by summing currents at the emitter node, the same process that led to **(5)** and **(6)**. **(6)** is repeated below with v_e replaced by its name in this analysis, v_o.

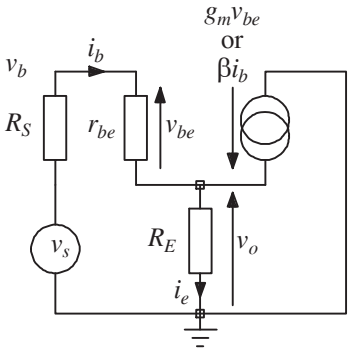

Figure 7

Small signal equivalent circuit of an emitter follower

$$v_o = v_{be} R_E \left(\frac{1}{r_{be}} + g_m \right) \approx v_{be} R_E g_m \qquad \textbf{(10)}$$

A second equation relating v_{be}, v_s and v_o is obtained by summing voltages around the input loop

$$v_s = i_b R_S + v_{be} + v_o = v_{be} \left(1 + \frac{R_S}{r_{be}} \right) + v_o \qquad \textbf{(11)}$$

and using the approximate result of **(10)** to eliminate v_{be} from **(11)** gives

$$\frac{v_o}{v_s} = \frac{r_{be} g_m R_E}{\left(r_{be} g_m R_E + R_S + r_{be} \right)} = \frac{R_E}{\left(r_e + \frac{R_S}{\beta} + R_E \right)} \quad \text{where } r_e = 1/g_m \,. \qquad \textbf{(12)}$$

The important conclusions are

- the gain is non-inverting
- the gain is very close to unity if $R_E \gg R_S/\beta$ and $1/g_m$, conditions that are usually satisfied.

The input resistance looking into the base terminal is as described for the common emitter with emitter degeneration in the analysis leading to **(9)**. The result is repeated here

$$r_i = \frac{v_b}{i_b} = r_{be} + (\beta + 1) R_E \qquad \textbf{(13)}$$

- the input resistance is dominated by the $(\beta + 1)R_E$ term.

The common base connection

Although sometimes used on its own, the common base connection is most commonly used in combination with other circuits - ie, as part of a multi transistor sub-circuit block. The circuit of a common base connected n-p-n device is shown in figure 8 and once again there is a p-n-p version of this circuit. It is assumed that any biassing resistances are included in R_S. Since I_C is large compared to I_B and $I_E = I_C + I_B$, the approximation $I_C \approx I_B$ is usually valid.

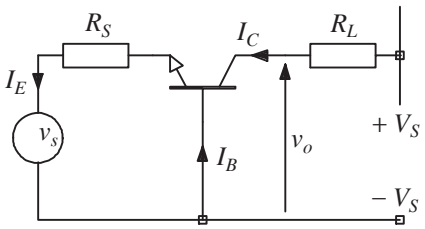

Figure 8

A common base circuit. The bias circuit is part of the thevenin resistance R_S.

The ss equivalent circuit is shown in figure 9. The effects of r_{ce} are neglected. The analytical process follows a similar pattern to the previous examples although the results are different. Start by summing currents at the emitter node,

$$i_s + i_b + g_m v_{be} = 0$$

or $$\frac{v_s - v_e}{R_S} + \frac{v_{be}}{r_{be}} + g_m v_{be} = 0 \qquad \textbf{(14)}$$

Note that $v_e + v_{be} = 0$ so $v_e = -v_{be}$ and this allows **(14)** to be rearranged to give v_{be} in terms of v_s,

$$v_{be} = -\frac{v_s}{R_S\left(\frac{1}{R_S} + \frac{1}{r_{be}} + g_m\right)} \approx -\frac{v_s}{1 + g_m R_S} \qquad \textbf{(15)}$$

since $1/r_{be} = g_m/\beta$ and $\beta \gg 1$.

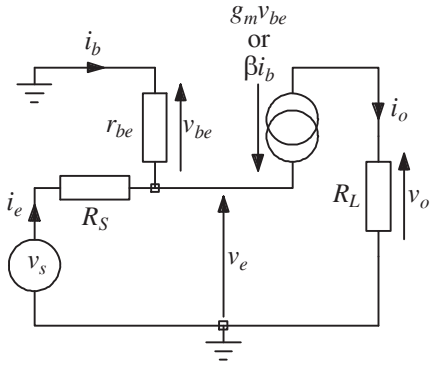

Figure 9

The small signal model of the circuit of figure 8. Note that r_{ce} is omitted from the model

At the output side

$v_o = i_o R_L = -g_m v_{be} R_L$ and combining this with **(15)** to eliminate v_{be} gives

$$\frac{v_o}{v_s} = \frac{g_m R_L}{1 + g_m R_S} = \frac{R_L}{r_e + R_S} \text{ where } r_e = 1/g_m. \qquad \textbf{(16)}$$

The important conclusions are

- the gain is non-inverting.
- gain is proprtional to R_L .
- If $R_S \gg r_e$ the gain is controlled by the ratio R_L/R_S.

The input resistance looking into the emitter of the transistor is given by

$$r_i = \frac{v_e}{i_e} = \frac{v_e}{\frac{-v_{be}}{r_{be}} - g_m v_{be}} \text{ but since } v_e = -v_{be} \text{ and } g_m \gg 1/r_{be} \text{ this reduces to}$$

$$r_i \approx \frac{1}{g_m} = r_e \text{ , a relatively low value (10s to 100s of Ohms).} \qquad \textbf{(17)}$$

Back to the simple op-amp of figure 1 . . . .

The parameters that we will work out here are overall gain and input resistance. The input resistance of the op-amp is essentially the first stage input resistance. The voltage gain of the op-amp is the voltage gain of the differential input stage multiplied by the voltage gain of the voltage amplification stage multiplied by the voltage gain of the output stage.

The input stage

The input stage circuitry is shown in figure 10. We must consider the effects of three transistors. T_1 and T_2 are the input differential pair and must be considered together and T_3 must be considered because its input resistance forms part of T_1's collector load resistance. If the input signal is regarded as v_{bT1} with respect to v_{bT2} (ie, v_{bT2} is taken as a signal ground), T_2 looks like a common base connection as far as T_1 is concerned and can be represented by its common base input resistance given by **(17)** as r_{e2} (= $1/g_{m2}$). The collector current of T_1 sees two resistors in parallel, R_1 and the input resistance of T_3. T_3 is a common emitter connection and its input resistance is given by **(4)** as r_{be3}.

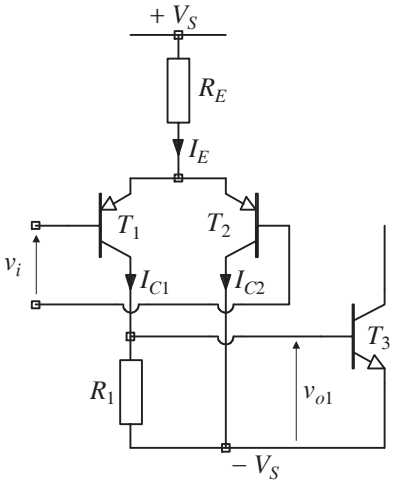

Figure 10

The circuit diagram of the input stage in the basic op-amp of figure 1.

A small signal equivalent circuit that embodies these representations of T_2 and T_3 is shown in figure 11. The circuit of figure 11 is the same as that of figure 5 with the exceptions that $R_S = 0$ and R_E and R_L become the parallel combinations $R_E//r_{e2}$ and $R_1//r_{be3}$ respectively. Since in figure 11 $R_E \gg r_{e2}$, the parallel combination $R_E//r_{e2} \approx r_{e2}$. Including these variable changes in **(8)**, the gain expression for figure 5, the voltage gain of the circuit of figure 11 is

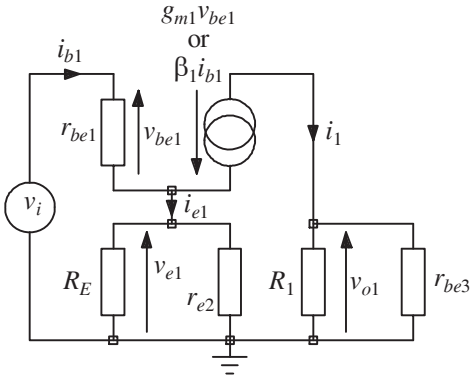

Figure 11

The small signal equivalent of figure 10. Note that T_2 has been replaced by its common base input resistance r_{e2} and that r_{be3} is in parallel with R_1.

$$\frac{v_{o1}}{v_i} \approx -\frac{R_1//r_{be3}}{r_{e1} + r_{e2}} \qquad \textbf{(18)}$$

- to maximise the gain of this circuit we need to make both R_1 and r_{be3} as large as possible.

It is tempting to think that we might also aim to reduce the $r_{e1} + r_{e2}$ term but remember that $r_e = 1/g_m$ and $g_m = eI_C/kT$. This means that to reduce r_e one must increase I_C. Since dc conditions demand $I_{C1}R_1 = 0.7$ V, an increase in I_{C1} would have to be accompanied by a decrease in R_1giving no net gain advantage. Input bias currents (I_{B1} and I_{B2}) would also be adversely affected.

The input resistance of the circuit of figure 11 is given by **(9)** remembering that in this case R_E must be replaced by r_{e2}

$$r_i = r_{be1} + (\beta_1 + 1)r_{e2} \qquad \textbf{(19)}$$

and if $I_{C1} \approx I_{C2}$ and $\beta_1 \approx \beta_2$, i.e., T_1 and T_2 are balanced and identical, $r_i \approx 2r_{be1}$.

The remaining stages are standard circuit shapes. The T_3 circuit is the standard common emitter circuit of figure 2. The base voltage is v_{o1} which was calculated (in terms of v_i) in the input section considerations that led to **(18)**. This means that $R_S = 0$ (because its effects were taken into account in the calculation of v_{o1}. The effective R_L is R_{VA} in parallel with r_{ce} of T_3, r_i of T_4 and r_i of T_5. In the circuit of figure 1, R_{VA} will be much smaller than r_{ce3}, r_{i4} and r_{i5} so the parallel combination $\approx R_{VA}$. The T_3 stage gain will thus be (from **(3)** with $R_S = 0$)

$$\frac{v_a}{v_{o1}} \approx - g_m R_{VA} \qquad \textbf{(20)}$$

The output stage, T_4 and T_5 are emitter follower circuits connected together in what is known as a double ended or push-pull arrangement. T_4 is an n-p-n transistor and is active during positive half cycles when current must flow from the positive power supply via T_4 to the load. T_5 is a p-n-p transistor and is active during negative half cycles when current flows from ground throught the load and T_5 to the negative supply. The emitter follower gain is very close to unity as shown by **(12)** and this leads to an overall amplifier gain

$$\frac{v_{o4}}{v_i} = \frac{v_{o4}}{v_a} \text{ x } \frac{v_a}{v_{o1}} \text{ x } \frac{v_{o1}}{v_i} = \frac{R_1 // r_{be3}}{r_{e1} + r_{e2}} g_m R_{VA} \qquad \textbf{(21)}$$

and for an amplifier circuit such as figure 1 this gain will be in the low thousands. A general purpose commercial op-amp will have a gain larger than this figure by a factor of two to three orders of magnitude. The next section looks at how the basic circuit of figure 1 can be refined to improve the gain and other parameters.

Refinements to the basic op-amp circuit of figure 1

Problems with the circuit of figure 1

Input stage

1 In the input stage, half the signal is wasted because the collector of T_2 is connected directly to the negative supply rail.

2 There is also a potential problem with collector current imbalance between T_1 and T_2 which will give rise to offset errors.

3 The input bias current is high and the input resistance is low in comparison with commercial general purpose op-amps.

4 The effective R_L of the first stage is relatively low leading to a very low gain.

T_3 stage

5 R_{VA} cannot have a large value because of the constraints imposed by dc conditions but a large value is desirable to maximise signal gain.

Output (T_4 and T_5) stage

6 the input resistance of T_4 and T_5 is dependent on the external op-amp load (effectively the R_E of the emitter follower of figure 6) and this has a direct bearing on voltage amplification stage gain.

7 The output resistance of the emitter follower is dependent on its source resistance.

8 The output transistors in figure 1 will give rise to severe crossover distortion. Crossover

distortion is distortion to the shape of the signal that occurs when conduction transfers from one output transistor to the other.

Solutions

Problems 1, 2, 3 and 4

Problems 1 and 2 are usually solved by introducing a circuit called a current mirror to form an active load for T_1 and T_2. There is a number of different current mirror circuits that have been devised but the one shown in figure 12 is the simplest and therefore the easiest to understand. The more complicated ones were devised to correct deficiencies in the basic circuit of figure 12. We will first look at the behaviour of current mirrors before looking at the current mirror - differential pair combination.

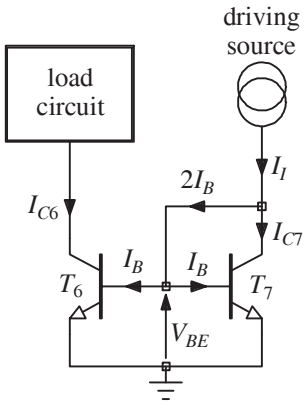

Figure 12
A current mirror circuit

T_6 and T_7 are assumed to be identical. The aim of the circuit is to draw from the load circuit the same current that is being driven into T_7 by the driving source. In other words, The circuit will ideally make $I_{C6} = I_I$. Notice that the collector and base of T_7 have been connected together and that the bases of the two transistors are connected together, as are the emitters. Thus V_{BE} will be the same for each transistor. I_I will set up a V_{BE} that is sufficient to make T_7 conduct a collector current $I_{C7} = I_I - 2I_B$.

$$I_I = I_{C7} + 2I_B = I_{C7}\left(1 + \frac{2}{h_{FE}}\right) \text{ or } I_{C7} = I_I \frac{h_{FE}}{2 + h_{FE}} \qquad \textbf{(22)}$$

Since V_{BE} is the same for both transistors, $I_{C6} = I_{C7}$ so **(22)** describes the relationship between input and mirrored current-s. Even with identical transistors the accuracy of the mirroring evidently depends upon the magnitude of h_{FE}. Note that in reality there will also be an error due to mismatch between the transistors but we will not pursue that error further here.

[The effect of finite h_{FE} can be reduced by adding a third transistor as shown in figure 13. This is sometimes called an h_{FE} helper transistor (or in some circles a β helper transistor). If we assume that all three transistors have the same h_{FE},

$$I_{BH} = \frac{2I_B}{h_{FE}} \text{ so } I_I = I_{C7} + I_{BH} = I_{C7} + \frac{2I_B}{h_{FE}} = I_{C7}\left(\frac{h_{FE}^2 + 2}{h_{FE}^2}\right), \qquad \textbf{(23)}$$

a much smaller error than that described by **(22)**.]

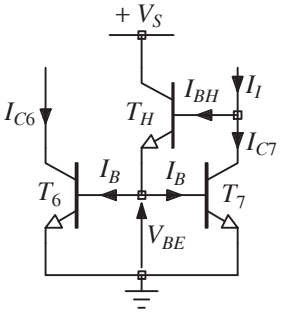

Figure 13
The current mirror of figure 12 with a helper transistor

The small-signal behaviour of the circuit of figure 12 is almost the same as the dc behaviour described by **(22)**. The differences are that for small-signal, h_{FE} is replaced by β and r_{ce}, the small signal resistance between collector and emitter, of T_7 will conduct a very small fraction of i_i, the small-signal equivalent of I_I, to ground. We will ignore this small loss of current. As far as the load is concerned T_6 looks like a current source in parallel with r_{ce6}.

Figure 14 shows the circuit diagram of the improved input stage circuit. The voltage amplification stage has been included because it has a significant effect on first stage gain. The

main cause of imbalance between I_{C1} and I_{C2} in figure 1 is the relatively high value of I_{B3}. In figure 14 T_8 is added to reduce this current which becomes I_{B8}. The combination of T_8 and T_3 is called a "Darlington pair". Most of I_3 flows through T_3 so $I_{B3} = I_3/h_{FE3}$ as before. I_{B3} forms the emitter current of T_8 so $I_{B8} \approx I_{B3}/h_{FE8}$. If the h_{FE}s of T_3 and T_8 are of the order of hundreds, the addition of T_8 reduces the bias current requirement of the voltage amplification stage by at least two orders of magnitude and I_{C1} is much closer to I_{C2} as a result.

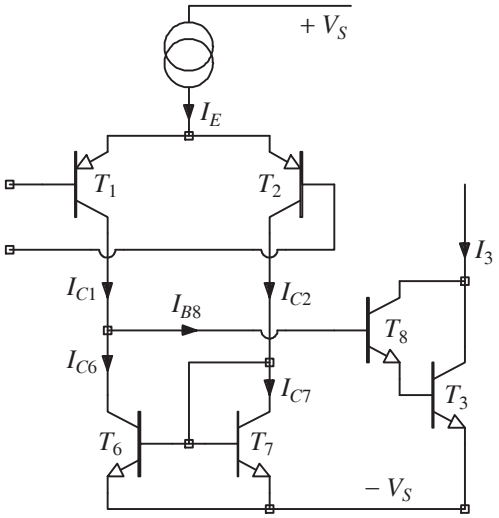

Figure 14
An improved input stage incorporating a current mirror and a Darlington pair

The Darlington pair of T_8 and T_3 also increases the input resistance of the voltage amplification stage. T_8 is an emitter follower connection with an effective R_E equal to the input resistance of T_3, r_{be3}. **(13)** gives the input resistance of an emitter follower and if the terms are modified for the circuit of figure 14, the input resistance looking into the base of T_8 is

$$r_{i8} = r_{be8} + (\beta_8 + 1)r_{be3} \qquad \textbf{(24)}$$

If the small-signal current gain of T_8 is in the hundreds, r_{i8} will be at least two orders of magnitude bigger than r_{be3}.

The addition of T_8 therefore helps to alleviate problems 2 and 3 and contributes to alleviating problem 4.

The current mirror also plays an important role in the input stage bias current balance and is also important from a signal point of view because the mirroring action works on ss changes as well as the static dc conditions. Consider the behaviour of the circuit of figure 14 when the voltage between the bases of T_1 and T_2 is zero. I_E splits between T_1 and T_2 to give collector currents of I_{C1} and I_{C2} respectively. The current I_{C2} instead of being returned directly to the negative supply as it is in figure 10 is now mirrored such that $I_{C6} \approx I_{C2}$. Assuming that the mirror is perfect, i.e, that $I_{C2} = I_{C6}$, a current sum at the collector node of T_1 gives

$$I_{C1} - I_{C6} = I_{C1} - I_{C2} = I_{B8} \qquad \textbf{(25)}$$

and assuming negligible base currents in T_1 and T_2

$$I_{C1} + I_{C2} = I_E \qquad \textbf{(26)}$$

Adding **(25)** and **(26)** gives

$$I_{C1} = \frac{I_E}{2} + \frac{I_{B8}}{2} \qquad \textbf{(27)}$$

and subtracting **(26)** from **(25)** gives

$$I_{C2} = \frac{I_E}{2} - \frac{I_{B8}}{2} \qquad \textbf{(28)}$$

Thus the collector currents of T_1 and T_2 are as balanced as they can be and if I_{B8} is small compared to I_{C1} and I_{C2} the mirror maintains an excellent balance.

When a signal is present at the input the split of I_E between T_1 and T_2 is modulated by the signal. Consider an instant when $V_{BT1} > V_{BT2}$. This will set up the conditions such that ΔI is taken from I_{C1} and added to I_{C2} to give

$$I_{C1} \rightarrow I_{C1} - \Delta I \quad \textbf{(29)}$$

$$I_{C2} \rightarrow I_{C2} + \Delta I \quad \textbf{(30)}$$

Using the I_{C1} and I_{C2} in **(27)** and **(28)** with the added current modulation of **(29)** and **(30)**, the modulated I_{B8} can be found by subtracting I_{C6} ($= I_{C2}$) from I_{C1}

$$I_{C1} - I_{C6} = \frac{I_E}{2} + \frac{I_{B8}}{2} - \Delta I - \frac{I_E}{2} + \frac{I_{B8}}{2} - \Delta I = I_{B8} - 2\Delta I \quad \textbf{(31)}$$

The mirror circuit has transferred all the collector current modulation in the differential input pair into a modulated I_{B8}. In addition, the effective load resistance seen by this node is a parallel combination of r_{i8} , r_{ce1} and r_{ce6}. r_{i8} has been shown to be large in **(24)** and r_{ce1} and r_{ce6} are intrinsically large. Together, the improvements offered by T_8 and the mirror improve the gain of the input stage by a factor of between 20 and 50 when compared with the circuit of figure 1. The inclusion of the mirror has contributed to problems 1, 2 and 4.

Problems 5 and 6

Problems 5 and 6 are related in the effect they have on the voltage amplification stage. The common emitter transistor, T_3, has a gain that is directly proportional both to its transconductance and to the load resistance seen between the collector node of T_3 and ground. In figure 1 this resistance consists of three main components:

- the collector emitter resistance of T_3, r_{ce3},
- the resistor R_{VA} and
- the input resistance of T_4 and T_5

The first of these is large and is difficult (though not impossible) to make larger. The second, R_{VA} is the most serious problem. The value of R_{VA} is determined by the dc condition requirements of the voltage amplification stage and this limits its value to a few 10s of kΩ. The difficulty is usually overcome by replacing R_{VA} by a current source, a strategy that raises the effective value of R_{VA} to the output resistance of the current source which usually approximates to the r_{ce} of the current source transistor. (The tail resistor, R_E, of the differential pair is also usually replaced by a current source so that I_E is largely independent of common mode input voltage.) The input resistance of T_4 and T_5 is affected by the external load connected to the op-amp and this tends to make overall gain a function of external load. This effect can be significantly reduced by the inclusion of an extra transistor, T_9, which is an emitter follower forming a Darlington connected pair with whichever of T_4 or T_5 is conducting. These modifications can be seen in figure 15. The input resistance of T_9 can be estimated by repeated use of **(13)** so assuming that T_4 is conducting its input resistance will be

$$r_{i4} = r_{be4} + (\beta_4 + 1)R_{L\,EXT} \quad \textbf{(32)}$$

where $R_{L\,EXT}$ is the op-amp's external load resistance. The input resistance of T_9 is then

$$r_{i9} = r_{be9} + (\beta_9 + 1)r_{i4} \quad \textbf{(33)}$$

The inclusion of the current souce load and T_9 will increase the voltage stage gain by at least an order of magnitude.

Problems 7 and 8

The problem caused by the input resistance that T_4 presented to the collector node of T_3 is also a problem from an output resistance point of view. If the output resistance of the emitter follower connected transistor of figure 6 is worked out, the result is

$$r_o = \frac{r_{be}}{\beta} + \frac{R_S}{\beta} = r_e + \frac{R_S}{\beta} \qquad \textbf{(34)}$$

Without T_9, the R_S for T_4 is the collector load for T_3 which has been made as large as possible to maximise gain. This would increase the output resistance of the amplifier. Including T_9 serves two purposes - it allows the input resistance of the output stage (T_9, T_4 and T_5) to be large and the output resistance of the output stage to be small thus simultaneously solving problems 6 and 7.

Problem 8 arises because T_4 will not start conducting until its base voltage ≈ 0.7 V and T_5 will not start conducting until its base voltage falls to ≈ -0.7 V. In figure 1 where the bases of T_4 and T_5 are connected together this leaves a region of signal between -0.7V and $+0.7$ V that is permanently lost. This problem is usually dealt with by the components R_9, R_{10} and T_{10} that have been added to figure 15. The effect of this circuit is to insert a fixed voltage source of 1.4 V between the bases of T_4 and T_5 so that when, for a rising signal, T_5 is about to stop conducting ($V_{B5} = -0.7$ V and $V_O = 0$V, T_4 is ready to take over conduction because at that point $V_{B4} = 0.7$ V. The R_9, R_{10}, T_{10} combination is maintained in a conducting state by I_4 which must be a few times larger than the peak current demanded by the base of T_5. The current through R_{10} can be worked out because there is 0.7 V across it. If the base current of T_{10} is negligible, the same current flows through R_9 so the voltage across the combination can be estimated.

Figure 15 shows the improved version of figure 1. The current sources I_{S1}, I_{S2} and I_{S3} exist to set up dc conditions by defining currents and this approach has the advantages described earlier. These current sources would normally be in the form of connected current mirrors with circuitry modified to allow the creation of well defined current ratios between the various sources. I_{S1} would typically be in a range 10 to 50 μA, I_{S2} in the range 100 to 200 μA and I_{S3} would be typically 1 to 5 mA.

The overall differential mode gain of figure 15 will be between two and three orders of magnitude larger than that of figure 1.

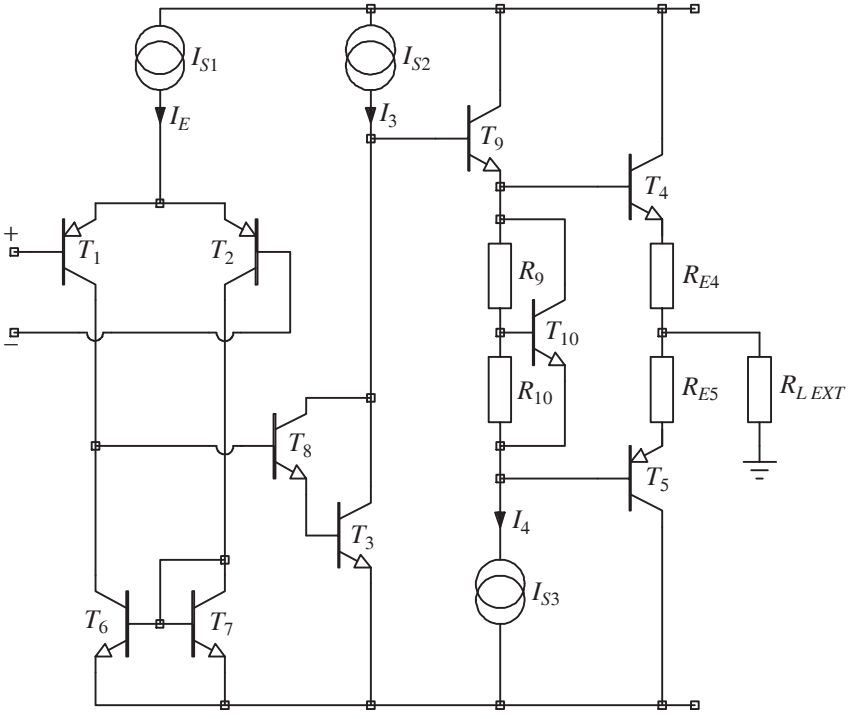

Figure 15

The circuit of figure 1 with improvements added. These improvements will increase the circuit gain be between two and three orders of magnitude