EEE225 Transistor Amplifier Circuit Analysis Problem Sheet

This problem sheet builds on the analysis of the two transistor amplifier circuits EEE118. It should prepare students well to tackle general problems involving transistors in analogue circuits. The circuits used in questions 1, 2 & 3 are not directly examinable, nor are questions 8 – 10. The techniques needed to solve the first few questions are the standard techniques of circuit analysis with active devices. These techniques were first introduced in EEE118 and are further developed in EEE225. If you can solve questions 1 – 3 confidently you'll have no problem at all with questions 4 – 7 which *are* examinable. Question 7 is quite similar to the sort of questions that come up in EEE223, and some parts of it to do with crossover distortion are in EEE225 as well.

How to tackle this sheet

Do question 1 or question 2 or question 3. Do *all* of questions 4, 5 & 6. Some of question 7 is needed in EEE225 especially related to crossover distortion, the rest is needed in EEE223.

If you feel that you've not had enough practice, go back and do the other questions as well. It would certainly be a good idea to look at the past exam papers as well for practice questions. You should find the exam questions much easier than the problems in this sheet, consiquently if you can do the sheet the exam should not pose any difficulty.

Questions 8 – 10 are for students who love the topic and want to go on an adventure of their own. The solution of these questions uses many of the techniques in this course but also moves outside the scope of the course. Unless you have lots of time available having done all the other quesetions and being up to date with all your other modules I would not devote time to these questions.

If you're looking for even more analogue try Gray, Hurst, Lewis and Meyer, which is considered by many to be the standard text on the subject. Behzad Ravazi has also written some very well liked books on the topic. He also has video lectures on YouTube which covers much of EEE118 and the semiconductors and analogue aspects of EEE225 https://www.youtube.com/watch?v=yQDfVJzEymI&list=PL7qUW0KPfsIIOPOKL84wK_Qj9N7gvJX6v

Question 1: A Common Emitter Circuit

This question is about the "type 1" common emitter circuit from EEE118. Unless otherwise stated, assume that all capacitors are short circuit in the mid-band. Some solutions will be easier to reach if R_L and R_C are lumped together as R'_L. Similarly R_B may be used to represent the parallel combination of R_1 and R_2.

The objective with the small signal derivations is to show which components are in control of certain circuit parameters, therefore the final form of the answer should be manipulated to reveal this information as clearly as possible. Arranging equations in a way that reveals certain underlying relationships in the circuit parameters is something computers are not very good at, this sort of work is best done by hand.

1. Find the DC conditions of the common emitter circuit in Figure 1 assuming the base current of Q_1 can be ignored.

2. Find the DC conditions again but taking into consideration the base current. Perform your calculations for the full range of h_{FE}. Find the range of h_{FE} from the Fairchild Semiconductor BC549 datasheet.

3. Explain (briefly, using bullet points for example) the job of each component in the circuit.

4. Explain (in words) why the emitter resistor, R_{E} acts to reduce the gain of the circuit unless it is decoupled by C_{E}.

5. Draw and label the small signal equivalent circuit for Figure 1.

6. Calculate the small signal transconductance, g_{m}, and base emitter resistance, r_{be} for the range of h_{FE} given in the Fairchild Semiconductor datasheet. You may assume that the transistor stage will be operated at frequencies considerably below the transition frequency, f_T, and therefore $\beta = h_{\mathrm{FE}}$

7. Show that the mid-band voltage gain of the common emitter circuit shown in Figure 1 is given by (1).

8. Show that the mid-band output resistance of the amplifier circuit in Figure 1 is given by (2).

9. Show that the mid-band input resistance of the amplifier circuit in Figure 1 is given by (3).

10. Show that the mid-band current gain given by (4).

11. Find an expression for the transresistance v_o/i_i of the amplifier stage shown in Figure 1.

12. Draw and label the small signal equivalent circuit for Figure 1 if C_{E} is *open* circuit at all frequencies of interest, all other capacitors may be considered short circuit.

13. Assuming C_{E} is *open* circuit at all frequencies of interest, derive the input resistance, output resistance, voltage gain and current gain of the amplifier. The final solutions take the forms shown in (5) - (8).

14. Given your solution for the small signal properties of the stage without emitter decoupling, determine what components are in control of the voltage gain, current gain, input resistance and output resistance. Comment on the effect of emitter degeneration on the small signal parameters. For example, which components are in control of the voltage gain? Which components dominate input resistance? What are the main components which reduce current gain?

15. State the numerical values of voltage gain, current gain, power gain, input resistance and output resistance with and without emitter decoupling over the range of h_{FE} given in the datasheet.

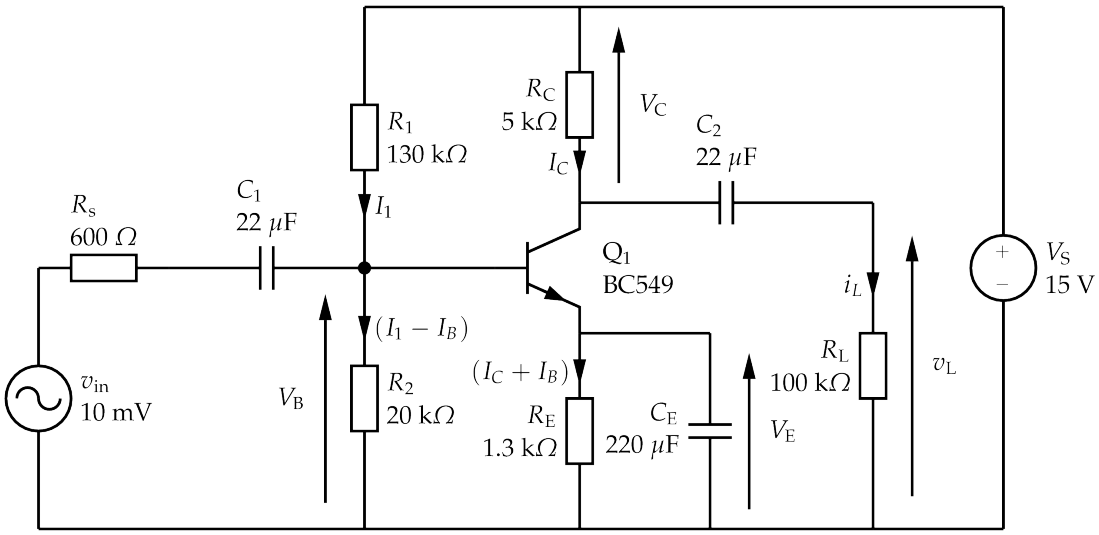

Figure 1: A common emitter amplifier circuit.

$$\frac{v_o}{v_i} = -\frac{g_m\, R'_L}{Rs\left(\frac{1}{R_B} + \frac{g_m}{\beta}\right) + 1} \tag{1}$$

$$r_o = \frac{v_o}{i_t} = R_C \tag{2}$$

$$r_i = \frac{v_i}{i_i} = \frac{1}{\frac{1}{R_B} + \frac{g_m}{\beta}} \tag{3}$$

$$\frac{i_o}{i_i} = \beta \frac{R_B}{R_B + r_{be}} \text{ or } \frac{\beta}{1 + \frac{\beta}{g_m R_B}} \tag{4}$$

$$\frac{v_o}{v_i} = -\frac{g_m R'_L}{R_S \left(\frac{1}{R_B} + \frac{g_m}{\beta} + \frac{1}{R_S} + \frac{(\beta+1)}{\beta} R_E g_m \left(\frac{1}{R_B} + \frac{1}{R_S} \right) \right)} \tag{5}$$

$$r_i = \frac{1 + \frac{\beta}{g_m R_E (\beta+1)}}{\frac{1}{R_B} + \frac{1}{R_E (\beta+1)} + \frac{\beta}{g_m R_E R_B (\beta+1)}} \tag{6}$$

$$r_o = R_C \tag{7}$$

$$\frac{i_o}{i_i} = -\frac{\beta}{\beta \left(\frac{1}{g_m R_B} + \frac{R_E}{R_B} \right) + \frac{R_E}{R_B} + 1} \tag{8}$$

Question 2: A Common Base Circuit

This question is about a capacitively coupled common base amplifier.

1. Find the DC conditions of the common base circuit in Figure 2 assuming the base current of Q_1 can be ignored.

2. Find the DC conditions again but taking into consideration the base current. Perform your calculations for the full range of h_{FE}. Find the range of h_{FE} from the On Semiconductor MJE340 datasheet.

3. Explain (briefly, using bullet points for example) the job of each component in the circuit.

4. Draw and label the small signal equivalent circuit for Figure 2.

5. Calculate the small signal transconductance, g_{m}, and base emitter resistance, r_{be} for the range of h_{FE} given in the Fairchild Semiconductor datasheet. You may assume that the transistor stage will be operated at low frequencies and therefore $\beta = h_{\text{FE}}$

6. Assuming the capacitors are short circuit at all frequencies of interest, show that the input resistance of the amplifier circuit in Figure 2 is given by (9).

7. Assuming the capacitors are short circuit at all frequencies of interest, show that the output resistance of the amplifier circuit in Figure 2 is R_C.

8. Assuming the capacitors are short circuit at all frequencies of interest, show that the transresistance (output voltage / input current) gain of the common base circuit shown in Figure 2 is given by (11).

9. Derive an expression for the current gain. Solution: (12).

10. Derive an expression for the voltage gain. Solution: (13).

11. Practical transistors have a physical resistance between the active part of the base region and the transistor package leg. This is partly made from the ohmic bond-wire resistance inside the package and partly made from the ohmic resistance of the semiconductor between the position at which the bond wire is attached to the semiconducor and the position of the active part of the base material. Draw the small signal equivalent circuit assuming that this base spreading resistance, r_b, appears in series with the base leg. C_1 is still short circuit at all frequencies of interest.

12. Re-derive your small signal results so far assuming taking into account the base spreading resistance. The results are shown in (14) - (17).

13. Reflect on and then qualitatively describe (i.e. in words) the effect of the base spreading resistance on the stage's small signal parameters. Comment on the similarity of the feedback provided by lifting the base node in the common base circuit with the effects of degenerating the emitter in the common emitter circuit.

14. State the numerical values of the small signal metrics of performance with and without the base spreading resistance over the range of β. You may assume that the amplifier is operated at a low frequency and therefore $\beta = h_{FE}$

$$\frac{v_e}{i_{in}} = \frac{1}{\frac{g_m}{\beta} + g_m + \frac{1}{R_E}} \tag{9}$$

$$\frac{v_o}{i_o} = R_C \tag{10}$$

$$\frac{v_o}{i_{in}} = \frac{g_m R'_L}{\frac{g_m}{\beta} + g_m + \frac{1}{R'_E}} \tag{11}$$

$$\frac{\frac{\beta}{r_{be}}}{\frac{1}{r_{be}} + \frac{\beta}{r_{be}} + \frac{1}{R'_E}} \approx \alpha \tag{12}$$

$$\frac{v_o}{v_i} = \frac{g_m R'_L}{\left(\frac{1}{r_{be}} + g_m + \frac{1}{R_s} + \frac{1}{R_E}\right)} \tag{13}$$

$$\frac{v_e}{i_{in}} \approx \frac{r_b}{\beta} + \frac{1}{g_m} \tag{14}$$

$$\frac{v_o}{i_{in}} = \frac{R'_L}{\frac{1+\beta}{\beta} + \frac{1}{g_m R'_E} + \frac{r_b}{R'_E \beta}} \tag{15}$$

$$\frac{i_o}{i_{in}} = \frac{1}{\frac{1+\beta}{\beta} + \frac{1}{g_m R'_E} + \frac{r_b}{R'_E \beta}} \tag{16}$$

$$\frac{v_o}{v_{in}} = \frac{g_m R'_L}{R_s \left(\frac{g_m}{\beta} + \frac{1}{R_s} + \frac{g_m r_b}{\beta R_s} + g_m + \frac{1}{R_E} + \frac{g_m r_b}{\beta R_E} \right)} \tag{17}$$

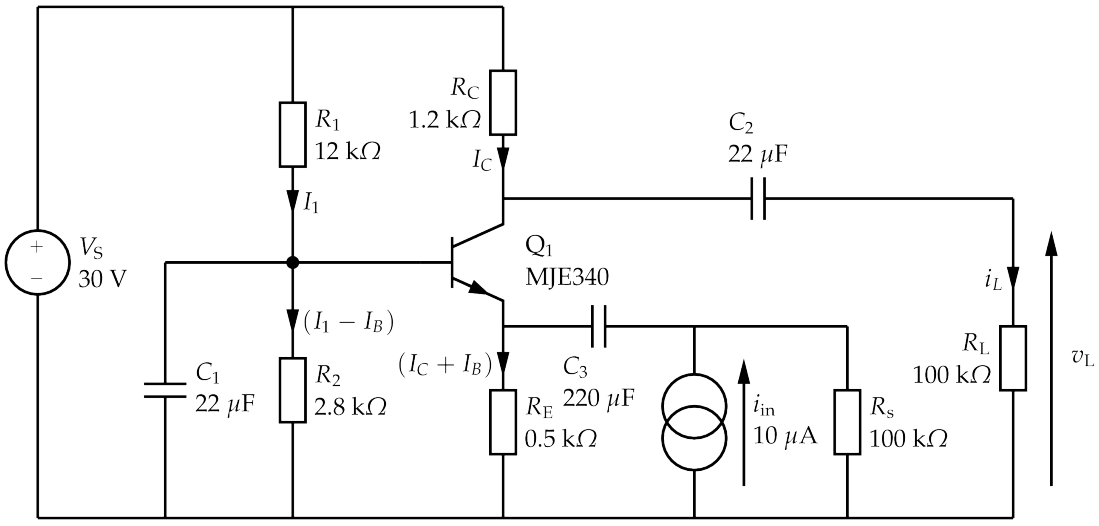

Figure 2: Common Base Amplifier Circuit

Question 3: An Emitter Follower Circuit

This question is about a capacitively coupled emitter (common collector) follower amplifier, shown in Figure 3. This emitter follower stage is used to drive a 16 Ω loudspeaker represented by R_E. The DC current biasing the stage also flows through R_E. This is often not practical but for the sake of making the question easier we will assume that this is a magical speaker (from my office...) that doesn't mind having a large DC component of current flowing through it. Of course the DC current dissipates power in the speaker but this would not be useful output power (sound) it would be heat. It would also hold the voice coil away from the center position but as we have said all these problems are ignored for the sake of simplicity.

1. Find the DC conditions of the emitter follower circuit in Figure 3 assuming the base current of Q_1 can be ignored. Choose V_B such that V_L, the emitter

voltage, is half way between the power supply and ground, thereby providing the largest possible output voltage swing.

2. Find the DC conditions again but taking into consideration the base current. Perform your calculations for the full range of h_{FE}. Find the range of h_{FE} from the On Semiconductor MJ15003 datasheet.

3. Explain (briefly, using bullet points for example) the purpose of each component in the circuit.

4. Sketch the output characteristic (V_{CE} *vs* I_C as a function of V_{BE} or I_B), add the operating point and the load line. On secondary axes, sketch the time dependent sinusoidal waveforms showing how the operating point moves according to the input signal, V_{in} and the output signal, V_L that results from this input.

5. Draw and label the small signal equivalent circuit for Figure 3.

6. Calculate the small signal transconductance, g_{m}, and base emitter resistance, r_{be} at the operating point for the range of h_{FE} given in the On Semiconductor datasheet. You may assume that the transistor stage will be operated at low frequencies and therefore $\beta = h_{\mathrm{FE}}$. Calculate the g_m and r_{be} at the maximum and minimum collector current based on the amplitude of the input waveform. Describe the effect will the variation of g_m and r_{be} have over the course of one cycle on the shape of the voltage and current waveforms in the circuit. To simplify your discussion you may assume β has no I_C dependence and that neither β nor g_m depend on temperature (or that the transistor will not get hot - same thing).

7. Based on the size of the input signal, the DC conditions you've calculated and your knowledge of electronic circuits, how valid is the small signal assumption in this case?

8. Assuming C_1 is short circuit at all frequencies of interest, show that the input resistance of the amplifier circuit in Figure 3 is given by (18). Comment on the size of R_s compared to the input resistance, what would you expect to find when evaluating the voltage gain of this stage.

9. Assuming C_1 is short circuit at all frequencies of interest, show that the output resistance of the amplifier circuit in Figure 3 is given by (19).

10. Assuming C_1 is short circuit at all frequencies of interest, show that the voltage gain of the circuit shown in Figure 3 is approximately unity.

11. Develop an expression for the current gain, determine its maximum value and the conditions required to reach that maximum.

12. Calculate the quiescent power dissipation in Q_1 and R_E.

13. Calculate the average power dissipated in the loudspeaker, R_L in one cycle if $R_s = 0.1\ \Omega$ and if $R_s = 600\ \Omega$. Qualitatively, do these figures relate to the earlier input resistance derivation?

14. Derive an expression for the instantaneous power dissipation in the transistor, Q_1. You may assume that the power dissipated in the transistor is the product of I_C and V_{CE} which will both vary *approximately* sinusoidally given a sinusoidal input. *Hint: this involves some integration of sines and cosines.*

15. Using your derivation find the input signal amplitude which results in the highest power dissipation in the *transistor*.

16. Show that the highest possible efficiency of this circuit is 25%. You may neglect losses in R_1 and R_2.

17. What is the conduction angle of Q_1? What class of operation is this stage operating in?

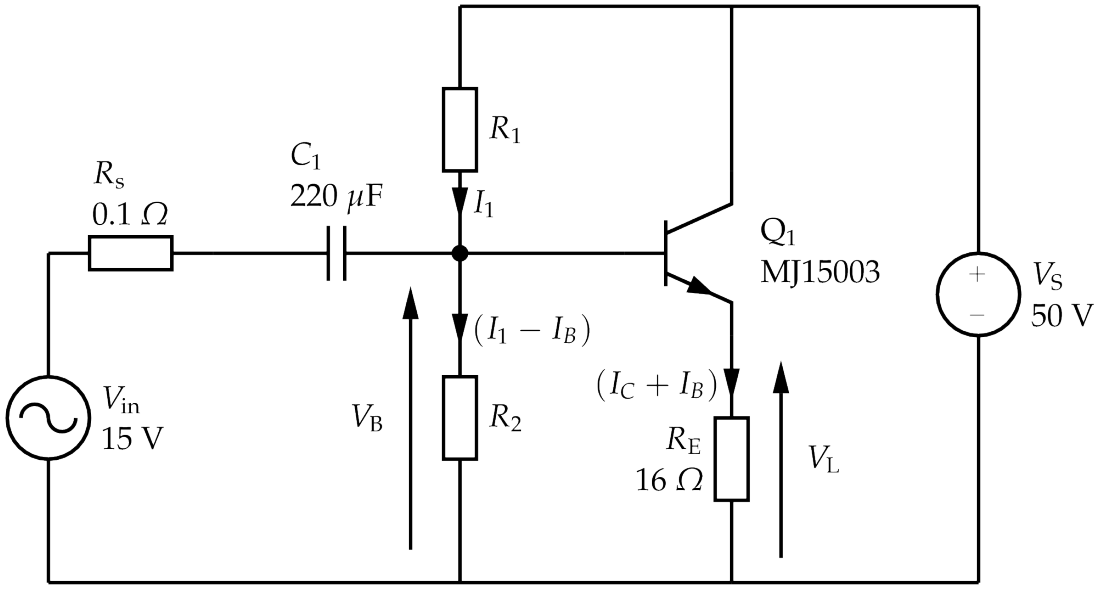

Figure 3: Emitter Follower Amplifier Circuit

$$r_{in} \approx R_B \tag{18}$$

where $R_B = R_1||R_2$.

$$r_o \approx \frac{1}{g_m} + \frac{R_B}{\beta} \tag{19}$$

Question 4: A Darlington Pair

One of the many problems with the circuit in question 3 is the very low input impedance. To ameliorate this a Darlington pair is often used in operational and discrete power amplifier output stages.

1. Re-draw Figure. 3 to make use of a Darlington pair. The upper transistor will be MJE340.
2. Design suitable component values to utilize the available rail voltage appropriately, include base current and the full range of h_{FE} in your calculations.
3. Explain briefly why the Darlington is an improvement.
4. Draw and label the small signal equivalent circuit for your circuit, you may assume that $R_B = R_1||R_2$ is very large compared to R_S and can be ignored.
5. Assuming C_1 is short circuit at all frequencies of interest, develop the input resistance of the Darlington emitter follower amplifier. You may assume that $R_B = R_1||R_2 >> R_S$ and therefore can be ignored. Attempt to find a form of your equation that can show the effect of N transistors cascaded. Comment on the effects of R_S on the stage voltage gain compared to the effects of R_S on the circuit in question 3.
6. Assuming C_1 are short circuit at all frequencies of interest, develop an expression for the output resistance of the amplifier. Similarly to the input resistance, try to arrive at a form of solution which shows the effect of N transistors in cascade.
7. Assuming the biasing network, $(R_B = R_1||R_2)$ can be ignored, derive an expression for the current gain.

Question 5: Widlar Current Mirror

The circuit in Figure 4 is a Widlar current mirror. The transistors are 2N5551. You may assume that the transistors are idential.

1. Show that the current in R_L is related to the current I_S by (20).
2. If I_S is 2000 μA what is the largest value R_L that can be used without pushing Q_1 into saturation? *Hint: you will need to use the datasheet to find* $V_{\text{CE(sat)}}$.

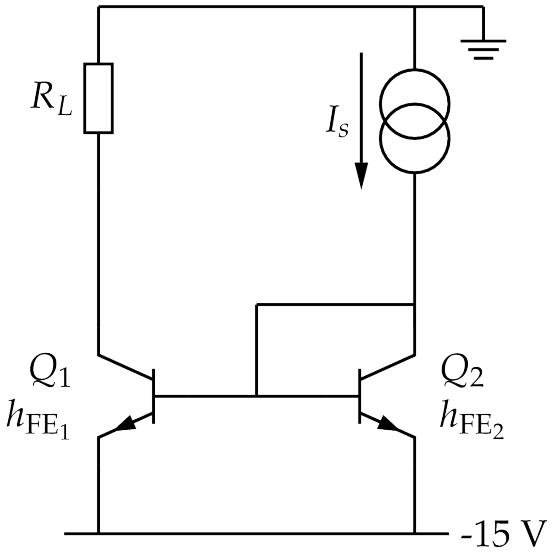

Figure 4: A Widlar current mirror circuit.

3. Draw the small signal equivalent circuit for the mirror, ensure you include r_{ce}.

4. Derive the output resistance of the mirror.

5. Derive the output resistance when emitter degeneration resistors are included.

6. By adding another transistor as in Figure. 5 a significant improvement can be made. What advantage does this circuit have over the two transistor mirror?

7. Derive the relationship between I_S and the load current in Figure 5.

$$\frac{I_S}{I_{R_L}} = \frac{h_{FE}+2}{h_{FE}} \tag{20}$$

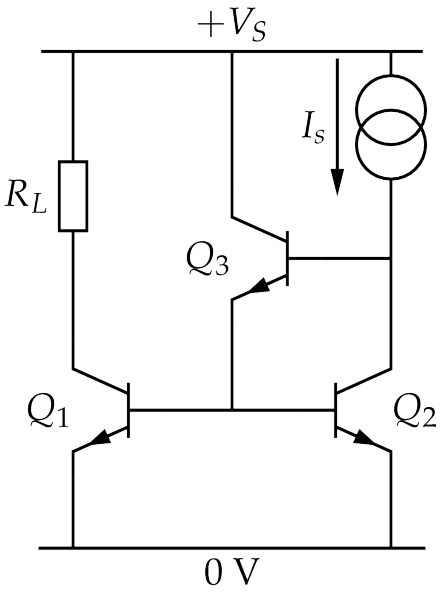

Figure 5: A current mirror circuit with helper transistor.

Question 6: Lin Style Operational Amplifier

There is a video solution to this question on the teaching resources website. The circuit of Figure 6 shows a simple form of op-amp circuit. Assuming that each transistor has a static current gain, I_C/I_B, and small signal current gain, $\Delta I_C/\Delta I_B$, of 100, that $kT/e = 0.026$ V and that each transistor has a V_{BE} of 0.7 V when conducting.

1. Estimate I_E, I_1, I_2 and I_3 assuming that $v_i = 0$ V, $v^+ = 0$ V, $v^- = 0$ V and $V_A = 0$ V.

2. Estimate the gain, v_{o1}/v_i, of the differential amplifier assuming that r_{ce} of Q_1 is very large compared to R_1. Remember to include the effects of Q_3 (ie, its input resistance) in your calculation.

3. Estimate the gain, v_a/v_{o1}, of the voltage gain stage assuming that r_{ce} of Q_3 and the input resistances of Q_4 and Q_5 are very large compared to R_{VA}.

4. Use your results from parts 2 and 3 to estimate the overall gain v_{o4}/v_i. What have you assumed in this calculation?

5. Using your powers of reasoning, identify which stage gain would be significantly improved if the small signal current gain of each transistor increased to 500.

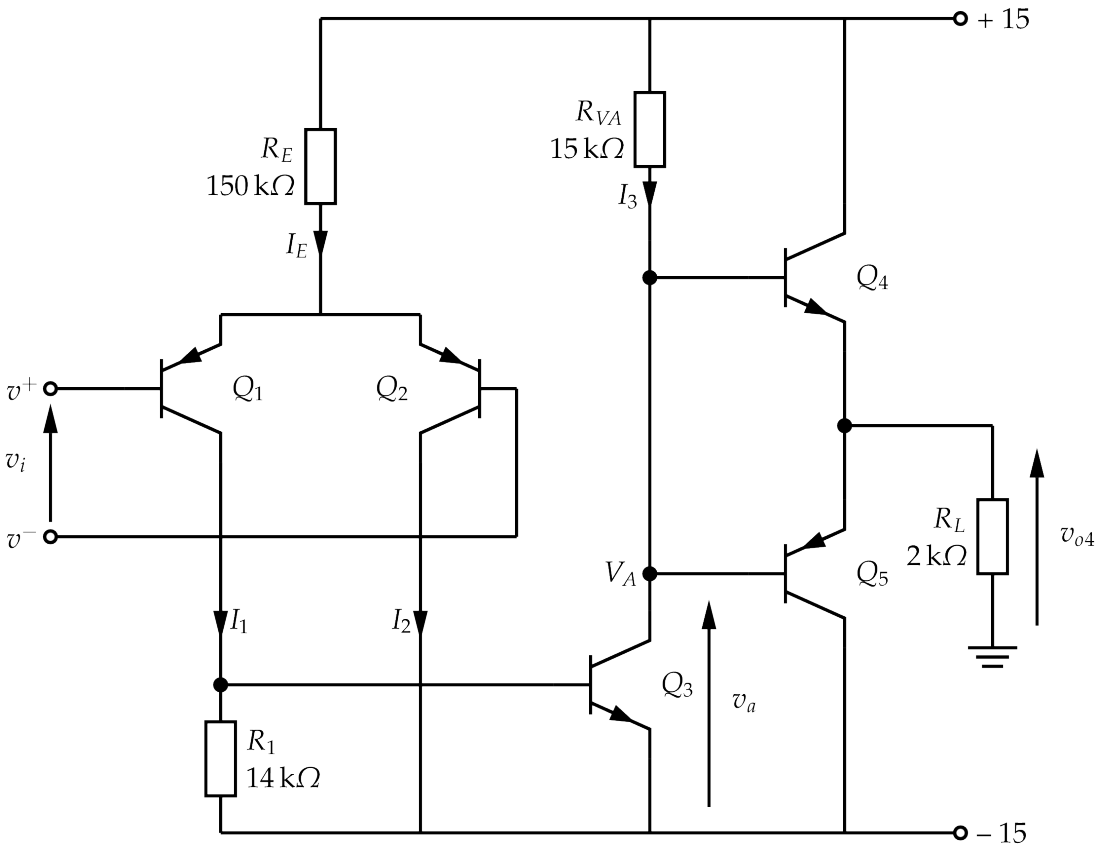

Figure 6: Simplified operational amplifier circuit.

Question 7: Push Pull Emitter Follower

1. Concisely describe the cause of crossover distortion in class B push-pull amplifiers.

2. Use a sketch to show the effects of crossover distortion on a triangle or sinusoidal waveform, taking particular care with your representation of the crossover region.

3. Sketch a circuit diagram of a voltage amplifier and push pull stage which largely overcomes the problems of crossover distortion and describe the operation of your circuit.

4. Calculate the quiescent power dissipation in one of the output transistors in your circuit.

5. Calculate the average power dissipated in the load resistor of your circuit.

6. Derive expressions for the instantaneous power dissipation in one of the output transistors. You may assume that the power dissipated in a transistor is the product of I_C and V_{CE} which will both vary *approximately* sinusoidally given a sinusoidal input. *Hint: this involves some integration of sines and cosines.*

7. Using your derivation find the signal voltage amplitude across the output which results in the highest power dissipation in the *transistor*.

8. Show that the highest possible efficiency of this circuit is approximately 70%.

9. The push-pull stage may operate in class C, B or A depending on the quiescent current flowing in the output transistors, which in turn is related to the voltage between the bases of the two output transistors. Sketch the load voltage and collector current waveforms of the two output transistors for each class, noting the salient features.

10. For each class of operation above, what angle of current conduction exists in each class and what *approximate* range of voltages must exist between the bases of the output transistors?

Question 8: Common Base Transimpedance Amplifier with DC servo

Download the journal paper at http://dx.doi.org/10.1088/0957-0233/23/12/125901. You may need VPN, see http://www.shef.ac.uk/cics/vpn for details. Describe how the transimpedance amplifier in Figure 6 of this paper works. Develop the DC conditions and the small signal parameters of the common base stage driven by the photodiode.

Question 9: A Charge Amplifier for X-Ray Detection

This question relates to a charge amplifier - its output votlage is porportional to the integral of the input current. This sort of circuit is often used to interface certain kinds of semiconductor detectors with signal processing hardware (such as multi-channel analysers). The circuit has a very high input impedace and low output impedance.

1. Describe in words how the circuit acts to stabilise its DC conditions. In so doing identify the circuit building blocks and describe the low frequency feedback (ignore C_3).

2. Calculate the DC conditions (currents through and voltages across all components (except C_3). Assume that for the JFET $I_D = 10$ mA at $V_{GS} = 0$ V. Assume the small signal current gain of all the BJTs is 100.

3. Postulate the purpouse of C_2. What is it likely to form a time constant with?

4. What is C_3's job in this circuit? It may help to think about the input as being short duration pulses of current sepperated by long periods of nothing. This would represent an x-ray generating a number of electron hole pairs as it passes through the detector, these become the pulse. The input impedance is very large so pushing current onto the gate will have to charge up or discharge some capacitors (including those internal to Q_1) the change in gate voltage will act to turn Q_1 on or off somewhat. This signal will propogate through the amplifier until it reaches the output (which is also the right hand side of C_3). Another way to look at it is to ask what will happen if I keep putting charge onto the gate and it doesn't leave. The amplifier will saturate, so how can I avoid this?

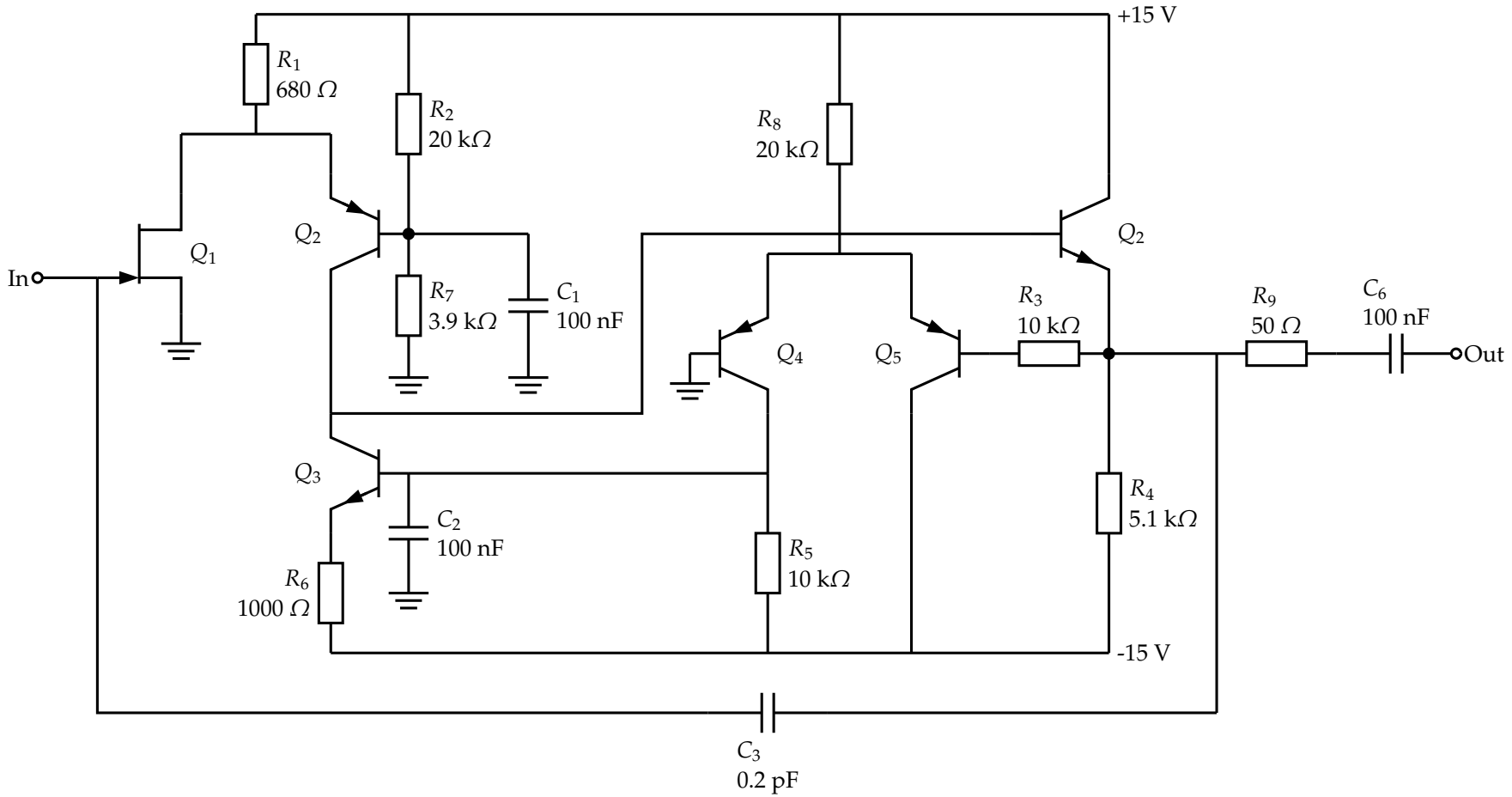

Figure 7: Akeel's charge amplifier.

Question 10: Three Transistor Amplifier with Singleton Input Stage

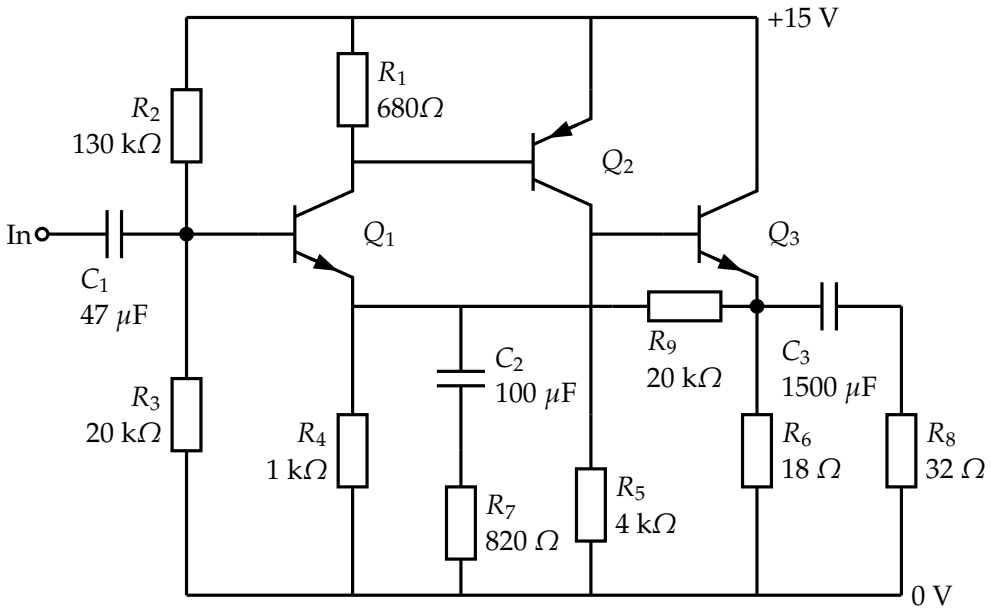

Figure 8: Simple opamp with "singleton" input and current feedback.

1. For the circuit in Figure 8, determine the DC conditions. For a purely analytical approach you will need to write out a system of equations and solve simultaneously. However since you are fleet of mind it is clear to you that this is basically a headphone amplifier therefore it will probably have equal voltage swing above and below the average value on its output. Hence you know that the Emitter of Q3 is likely to be at about 7.5 V. It is now soluble with no equations except Ohm's law.

2. approximate the input resistance (do not derive it, use your engineering brain to make a single calculation that leads you to a value with +/-10% accuracy).

3. What is the gain at DC (It is AC coupled but that does not mean there is no gain at DC).

4. What is the gain in the midband (AC gain, all capacitors short circuit).

5. list the major problems with the circuit and explain how they arrise. Why are real amplifiers not made like this? Think about input and output impedance, gain, distortion etc.

6. If you could only change one thing to improve the performance of the circuit what would it be?

7. how hot is Q3 likely to get if it is a 2N3055 in a TO3 metal package without a heatsink, is that acceptable? Why?

8. I described it as series–shunt feedback what does that actually mean? What impact does the 'mode' of feedback have on the circuit performance? (You will need to do some serious background reading in Grey Hurst Lewis and Meyer - it's to do with input and output impedance).

9. Since you've got Grey open...probably around page 583 if you're in the 5th edition. Teach yourself how to use signal flow graphs to analyse circuits with feedback. Apply the technique to the circuit in this question.

10. Replace the input transistor with a JFET, 2N3819. Re-design the circuit to perform the same function. The input stage biasing resistors can be removed and the gate of the JFET can float at 0 V.

11. Use LTSPICE to compare the input impedance of the two circuits.

12. Use the LoopGain2.asc example file in the "Educational" directory of LTSPICE to assess the open loop gain of this amplifier. Add compensation between collector and base of Q_2 observe the effects of changing the dominant pole frequency on the open loop gain for several values of capacitor (try 100 pF to start). Inspect the *open loop* gain and phase margins, compensate it to ensure stability.