EEE225: Analogue and Digital Electronics

Lecture VI

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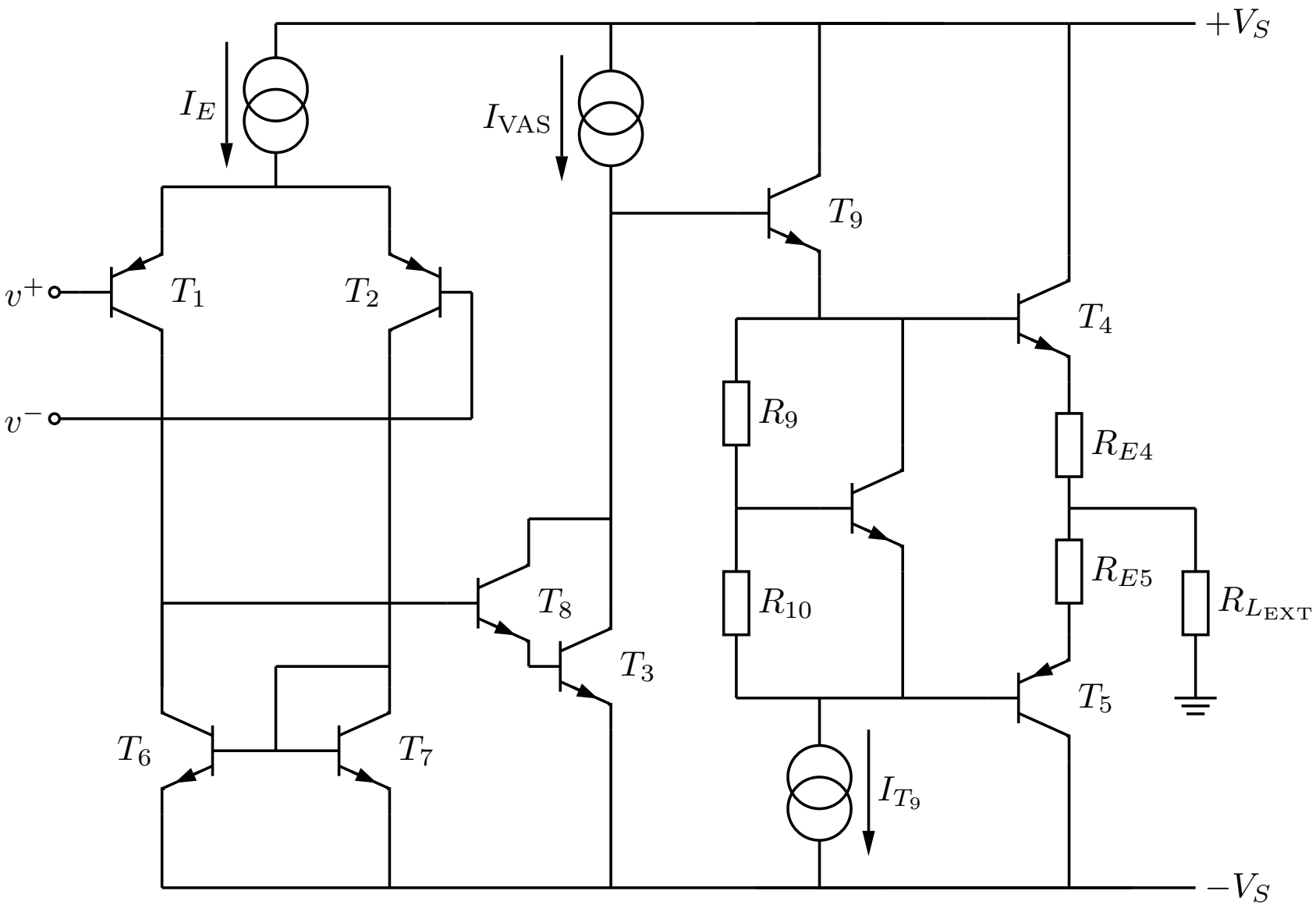
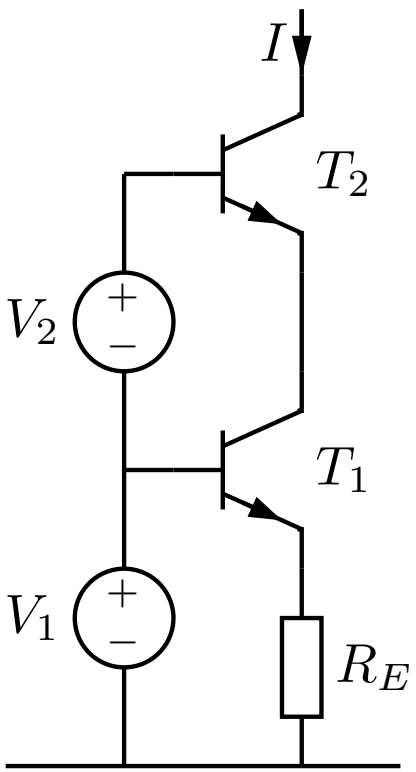
This Lecture


$+V_S$
I_E
I_{VAS}
T_9
v^+
T_1
T_2
T_4
v^-
R_9
R_{E4}
T_8
R_{E5}
$R_{L_{\text{EXT}}}$
R_{10}
T_3
T_5
T_6
T_7
I_{T_9}
$-V_S$

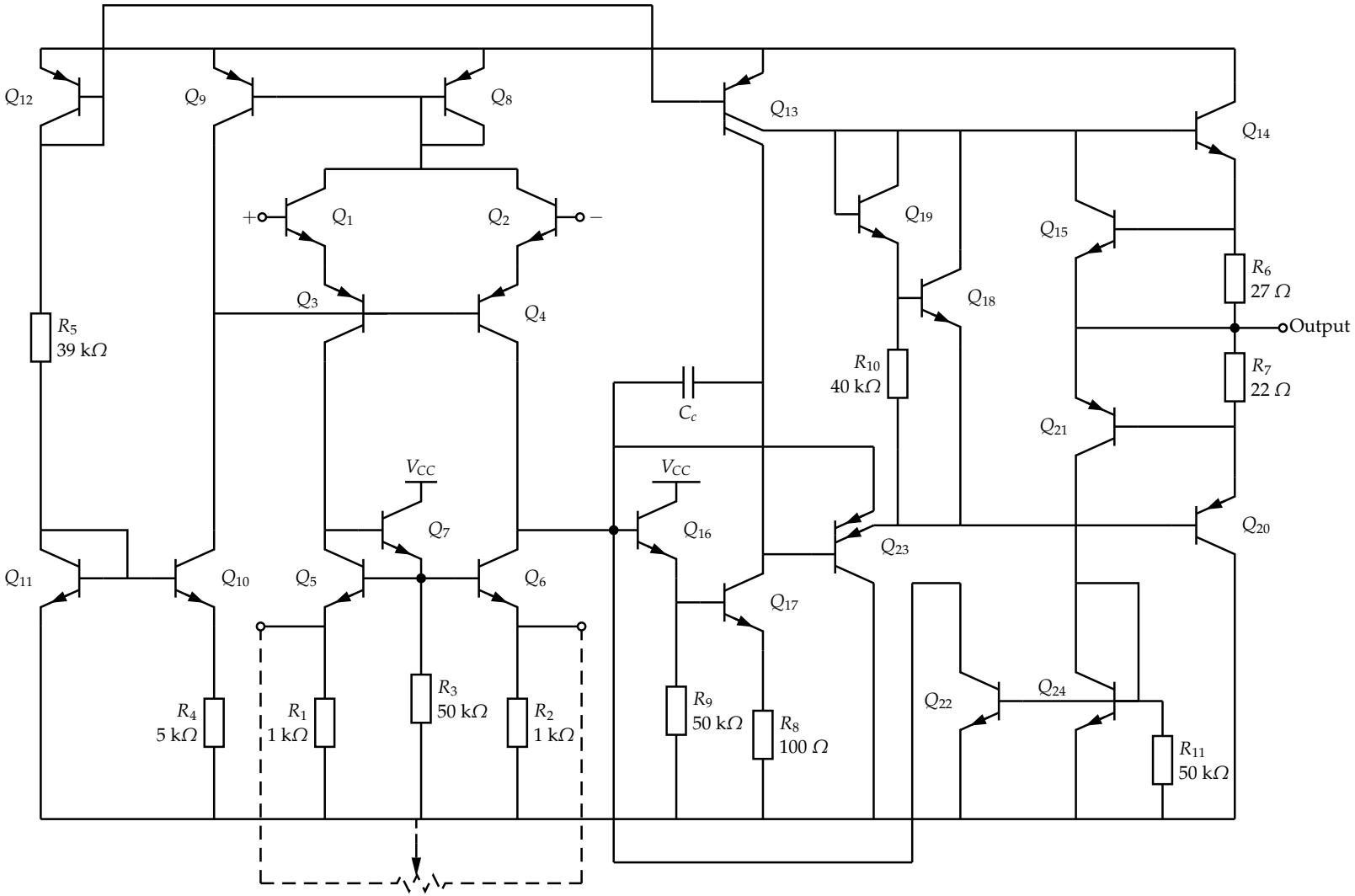
- I_E, I_{VAS} and I_{T_9} set up the DC or quiescent conditions by defining currents.
- Current sources are normally current mirror circuits with one or two additional components to set the DC conditions. The simple current source tends not to see much use.
- The current mirrors can be connected together to allow the ratio of supplied currents to be set. The simple current source has no similar advantage.
- I_E is typically $10 - 50\ \mu\mathrm{A}$. I_{VAS} is typically $100 - 200\ \mu\mathrm{A}$ and I_{T_9} is typically $1 - 5\ \mathrm{mA}$
- This improved circuit reduces all of the problems. However it is one possible implementation of a simple opamp. Real opamps tend to be somewhat more complicated.
- Notice the general lack of resistors - transistors are easy to produce in ICs, resistors (especially precise values) are difficult and expensive. Designers will always use one or more transistors if possible.

- A common emitter amplifier (T_1) connected to the input of a common base amplifier (T_2).
- Prevents voltage swing on the collector of (T_1) by making the resistance looking into T_2's emitter small.



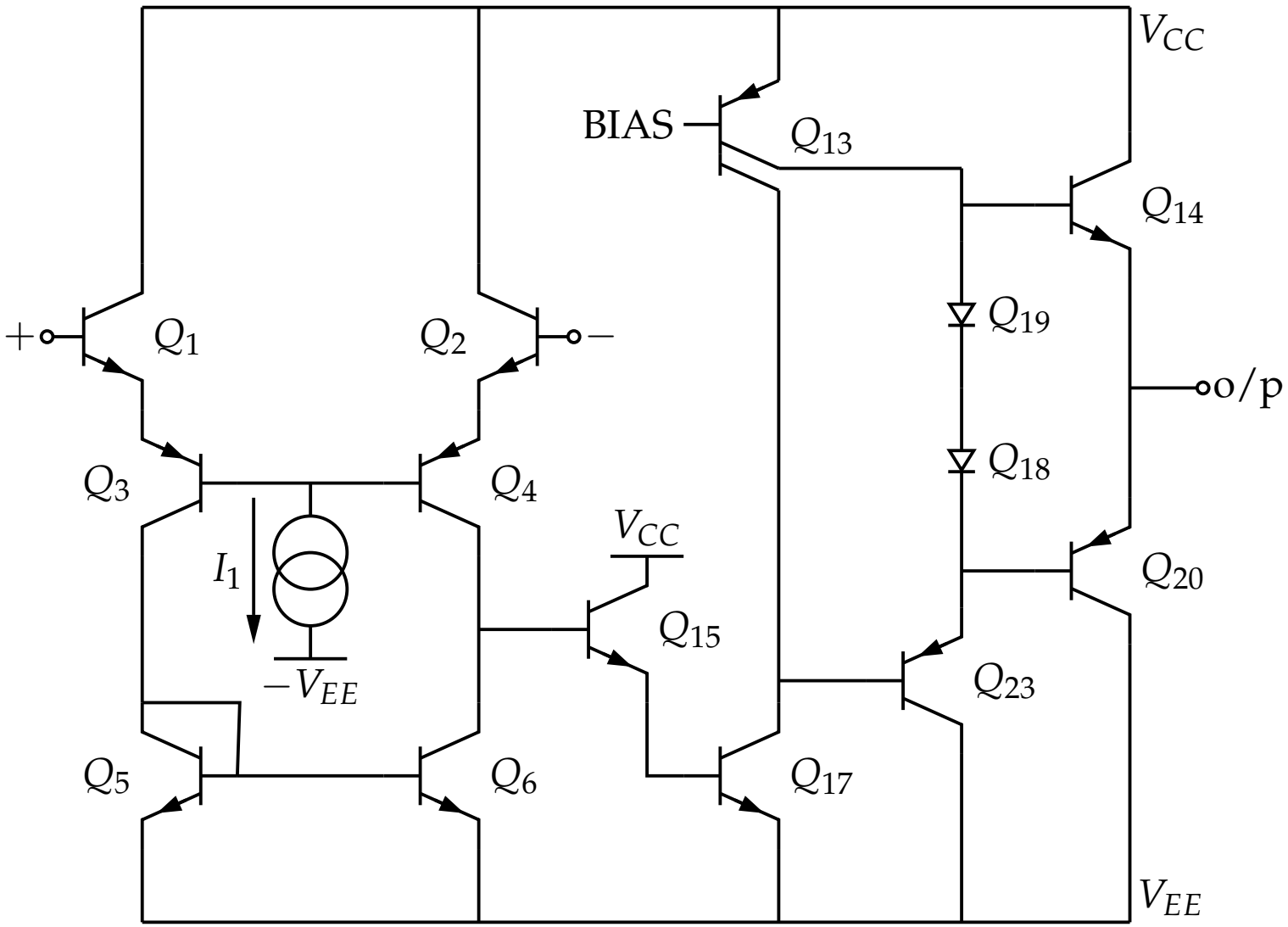
- Enhances the bandwidth of the CE stage by reducing the "Miller effect".
- Depletion capacitance of T_1's reverse biased CB junction couples signal voltages from the collector to the base developing undesirable negative feedback effect – overcome by preventing significant voltage swing on this node.
- The voltage swing on T_2's collector is OK because T_2's base is a fixed voltage - it does not have the input signal on it and is a low resistance path to ground for signals.

"Full" 741 Schematic[1]



[1] A little history: http://goo.gl/SpvgZL

Simplified 741



Qualitative 741 Description I

- The input transistors Q1 and Q2 are emitter followers that maintain high input resistance, and low input current.
- Q1 and Q2 drive Q3 and Q4 which are a *common base* differential pair of pnp transistors.
- Q5 and Q6 are a current mirror that actively loads Q3 and Q4.

These six devices perform three key functions of an opamp.

1. They provide the differential input with high r_{in}, with high CMRR and some gain. A little gain in the input stage is desirable from a noise and offset perspective.
2. Level shifting. pnp transistors in standard bipolar IC tech. are slow[2]. We would like to use only npn, but this limits the available output voltage. In the 741 lateral pnps Q3 and Q4 are placed in the signal path, their emitter is near the input voltage but their collectors are almost on the negative rail.

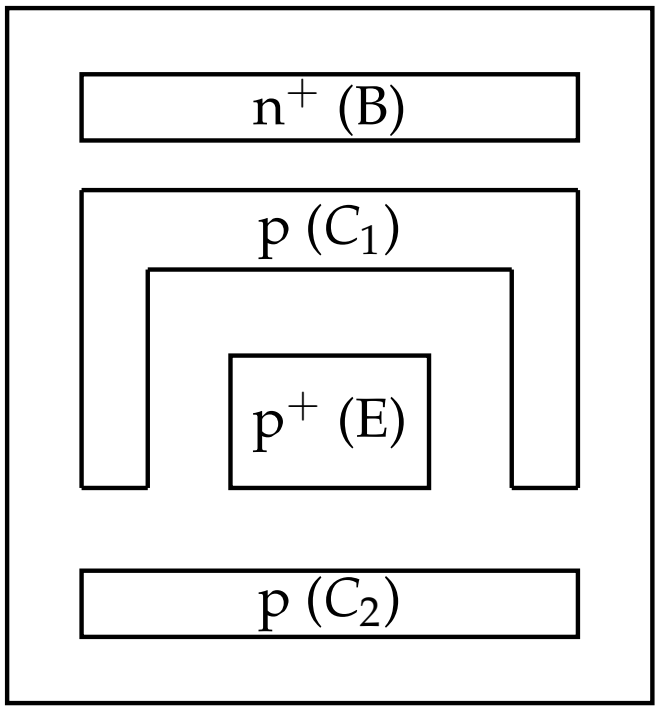
[2] Gray, Hurst, Lewis & Meyer, 4th Ed. Section 2.5.2.

Qualitative 741 Description II

1. Differential input and single ended output. Most modern opamps are differential input single ended output. A simple approach would be to take the output from Q3's collector and resistively load the Q3 & Q4 pair but this lowers the differential pair gain and lowers cripples the CMRR therefore the active load (current mirror) of Q5 and Q6 are used.

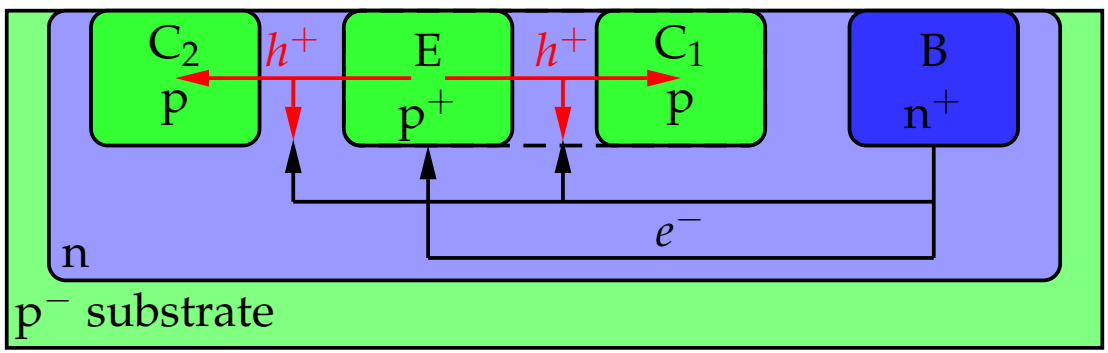
- Q16 is an emitter follower (Q16 and Q17 are *not* a Darlington pair). Q16 stops Q17 loading Q4's collector appreciably.
- Q17 is a common emitter amplifer actively loaded by Q13. Q17 provides most of the voltage gain.
- Q23 is also an emitter follower which mitigates the loading effect of the ouptut stage on Q17's collector.
- Q14 and Q20 are a push-pull Class AB output stage (a pair of npn and pnp emitter followers) which provides current gain and a low output impedance.

Dual Electrode Transistors[3,4]



- Q13 is a two collector latteral pnp.

- Collector ring split into two. One facing 3/4 of the emitter the other 1/4 of the emitter.
- essentilly two transistors that share a base and emitter where the saturation current, I_s, is split in the ratio of the collecting area.



[3] IC taredown with pictures at: http://goo.gl/KMNFnW
[4] Camenzind, "Designing Analog Chips", www.designinganalogchips.com

Frequency and Time Domain Limitations of Opamps

In this part of the course we will consider some (but not all) non-idealities of opamps. We will consider the opamp as having an *intrinsic* frequency response and this response will be *first order*. In the frequency domain, we will,

- Introduce the concept of a frequency response.
- Make use of the Bode plot to illustrate the frequency response.
- Discuss the practical significance of poles and zeros.
- Introduce the gain bandwidth product as a measure of small signal performance for an Opamp.
- Briefly touch on the Miller transform.

In the time domain, we will,

- Introduce the idea of slew rate limiting for sine and triangle wave-shapes.

Opamps with Frequency Dependent Feedback

In this part of the course we will consider some circuits which have feedback formed from capacitors and resistors. These circuits will be limited to *first order* problems.

- Integrator circuit
- Differentiator circuit
- Pole-zero circuits

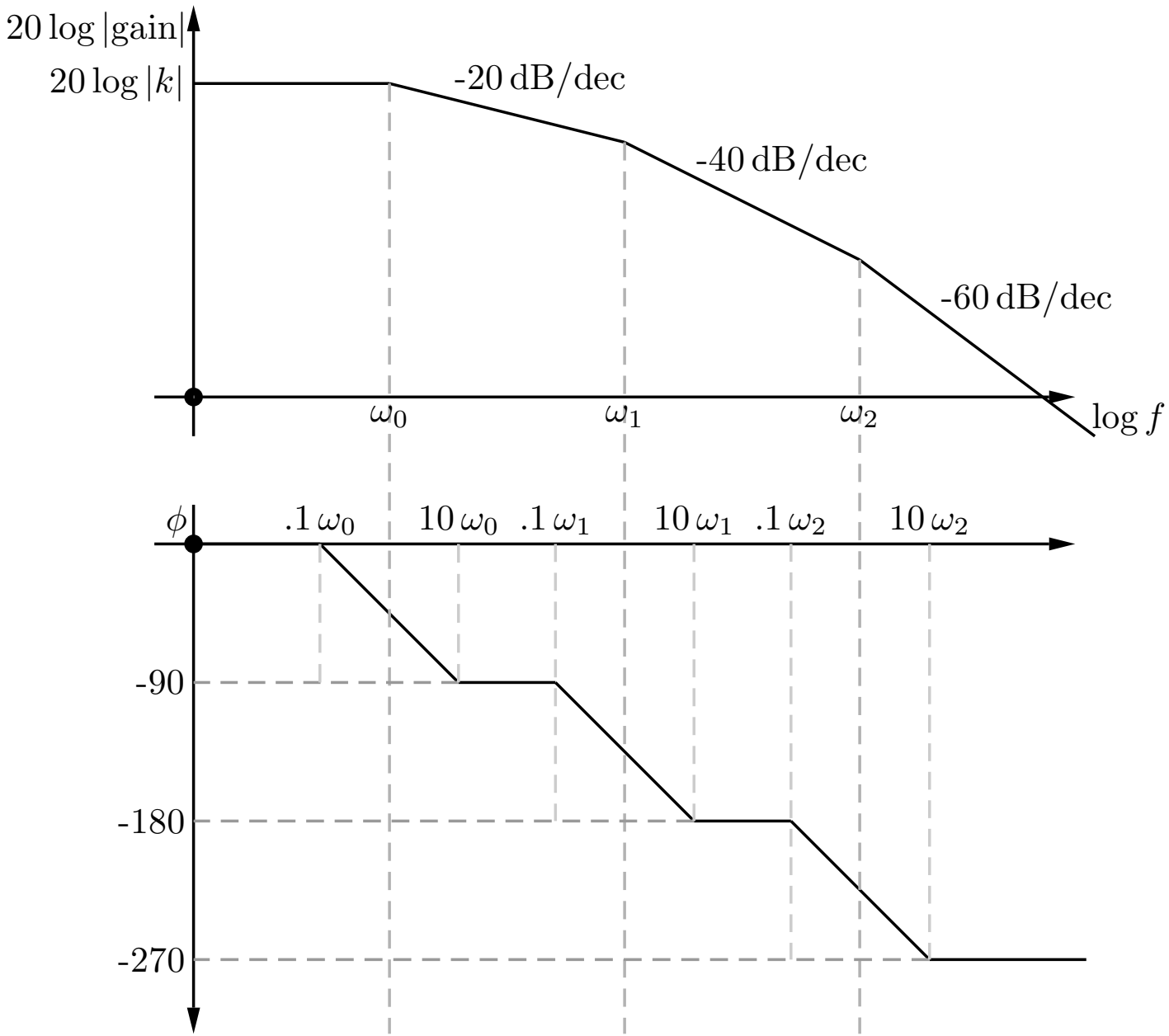
Opamp circuits having higher order feedback, or having first order feedback and a first order intrinsic frequency response (making them second order) are discussed in EEE224 or EEE227 and include second order passive circuits, some types of oscillator, Butterworth and Cheblychev (among other) filters and other non-linear and trans-linear circuits such as mixers and PLLs.

Opamp Intrinsic Frequency Response

- In EEE118 we always assumed A_V was ∞ or a constant real value.
- Making the open loop gain frequency dependent is a way of expressing the intrinsic frequency response of the opamp.
- In EEE225 we assume that A_V is first order, low pass response. Many opamps are designed to "look" first order.
- This design choice is made in order that engineers find opamps easy to work/design with (amplifier lab...).
- To see what effect this design choice has on the performance we will first assume that the opamp is 3rd order.

$$A_v = k \cdot \frac{1}{1 + j\frac{\omega}{\omega_0}} \cdot \frac{1}{1 + j\frac{\omega}{\omega_1}} \cdot \frac{1}{1 + j\frac{\omega}{\omega_2}} \tag{1}$$

in which k is the frequency independent part of the open loop gain, A_0, and ω_0, ω_1 and ω_2 are the frequencies of three real poles. The lowest is the dominant pole.

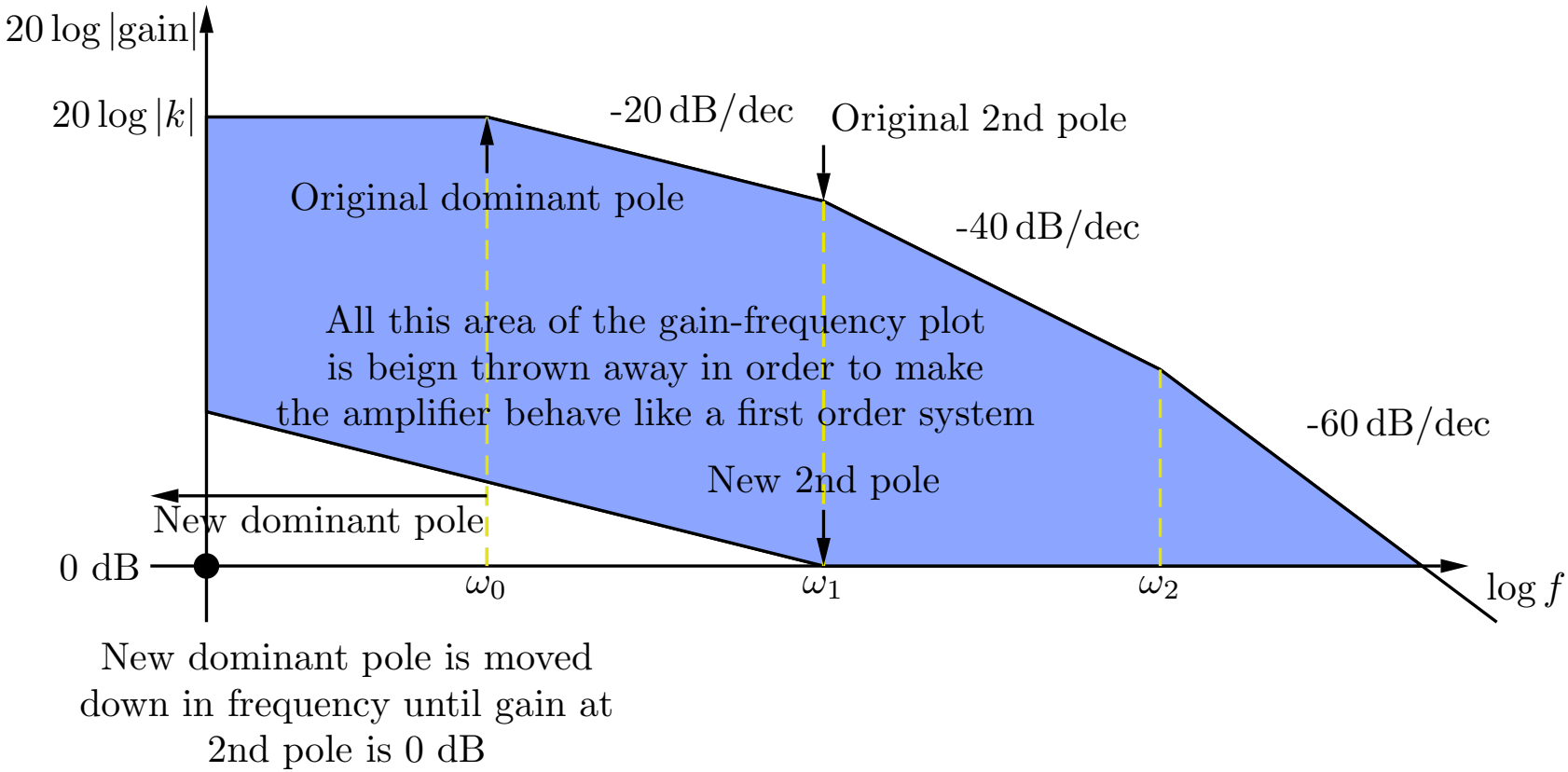

20 log |gain|
20 log |k|
-20 dB/dec
-40 dB/dec
-60 dB/dec
ω0
ω1
ω2
log f
φ
.1 ω0
10 ω0
.1 ω1
10 ω1
.1 ω2
10 ω2
-90
-180
-270

Reading the Bode Plot

Passing a pole when moving from low to high frequencies...

- yields an additional 20 dB/decade roll-off (decrease in amplitude)
- yields an additional 90° phase lag.
- The phase lag at the pole frequency will be 45°.
- The amplitude at the pole frequency will be -3 dB less than the low frequency value.
- The effects of phase shift will extend approximately 10× above and below the pole frequency.

Passing a zero when moving from low to high frequencies yields the same effects but amplitude increases and phase leads. All other points are valid.



The dominant pole is moved down in frequency (sometimes called "slugging") until the 2nd pole frequency is at the unity gain point (0 dB). The blue area is open loop gain which is *lost*.

Review

- Introduced the cascode circuit
- Briefly discussed three simplified schematics of some real opamps.
- Introduced the second section of the course (it's about opamps...)
- Described the open loop gain with a frequency dependence for the first time
- Reminded ourselves how to read a Bode plot
- Discussed how the higher order opamp is made to "look" first order