The University of Sheffield

Department of Electronic and Electrical Engineering

EEE118 Problem Sheet

Rectifiers and Smoothing

Note: All a.c. voltages are r.m.s. quantities unless otherwise stated and unspecified frequencies are 50Hz.

Q1 In the half wave rectifier circuit of figure 1 both the diode and the transformer are ideal (ie, *D* conducts with zero voltage drop for forward bias and is an infinite resistance for reverse bias and the transformer has zero series resistance).

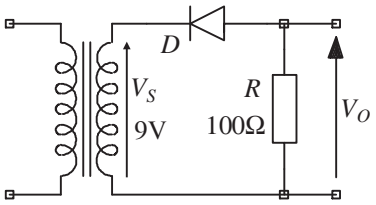

Figure 1

(i) Sketch the shape of the voltage V_O as a function of time for at least one period of V_S.

(ii) What is the peak value of V_O? (-12.73V)

(iii) What is the average value of V_O? (-4.05V)

(iv) What is the r.m.s. value of V_O? (6.36V)

(v) What is the power dissipated in *R*? (405mW)

If the transformer has a total effective resistance of 10Ω in series with its secondary winding.

(vi) What is the new peak value of V_O? (-11.57V)

(vii) What is the new power dissipated in *R*? (335mW)

Q2 What value of smoothing capacitor is required across the 100Ω load of figure 1 in order to achieve a ripple voltage of 0.3V peak to peak? What assumptions have been made in order to arrive at an answer? Estimate the power dissipated in the 100Ω load with this value of *C* connected. Assume that transformer and diode are ideal. (8500mF, 1.58W)

Q3 For the circuit of figure 3 what are the peak values of the voltage differences:

(a) $V_B - V_A$? (25.5V)

(b) $V_A - V_C$? (25.5V)

(c) $V_C - V_B$? (-51V)

Is the rectifier a full wave or a half wave type? *Note: The answers given ignore the diode forward voltage drop.*

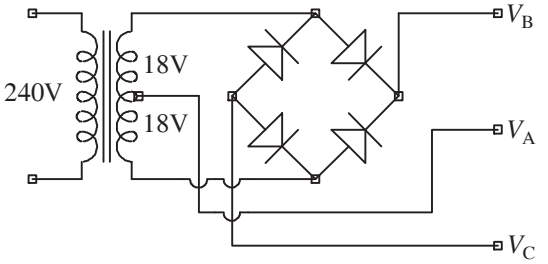

Figure 3

Q4 The circuit of figure 3 is to be used to supply an amplifier which requires nominally balanced positive and negative power supplies with respect to zero. The amplifier demands a current of 2A and at this current the ripple voltage must be less than 1V pk to pk on each supply rail.

(i) Redraw the circuit to include the capacitors necessary for capacitor input filtering of the rectifier output.

(ii) Estimate a suitable value for each capacitor. (20mF)

(iii) What d.c. component of output voltage will the smoothed supply provide? (24.3V)

(iv) What peak reverse voltage (PIV) must the diodes be capable of handling if reverse breakdown is to be avoided? (51V)

*The answer to part **(iii)** will be very dependent on the assumptions and approximations made. Assume here that all components used are ideal.*

Q5 The preamplifier section (tone controls etc) of the amplifier of question 4 requires a +10V supply at a current that may vary between 20mA and 50mA. This supply is to be derived from the main supply worked out in question 4 using a resistor and a zener diode.

(i) What zener breakdown voltage is required? (10V)

(ii) What value of series resistance is required if the current through the zener diode must be a minimum of 10mA? (230Ω)

(iii) What power rating must the zener diode have if a worst case condition is the disconnection of the preamplifier from its supply? (600mW)

(iv) What power rating must the resistor have if a worst case condition is the short circuiting of the preamplifier supply? (2.72W)

(v) What are the normal operating power dissipations in the resistor and zener diode? (980mW and 400mW respectively - when I_L can vary, worst case normal operating dissipations must be used)

(vi) What is the maximum zener diode slope resistance, r_Z , that can be tolerated if the pk to pk ripple voltage on the preamplifier supply must be ≤ 10mV? (2.3Ω)

AND FOR EXPERTS

Q6 The circuit of figure 6 is sometimes called a full wave voltage doubler. *(The diode clamp - peak detector combination is sometimes called a half wave voltage doubler)*

(i) Sketch the shape of V_O that you would expect to observe, taking special care with the ripple.

(ii) If $V_S = 20\text{V}, I_L = 100\text{mA}$ and the components are ideal, what value of C_1 and C_2 is necessary if the peak to peak ripple must be 5V or less? (400μF)

(iii) What is the average V_O under the conditions of part **(ii)**? (51.6V)

(iv) What PIV must D_1 be able to withstand? (54.1V)

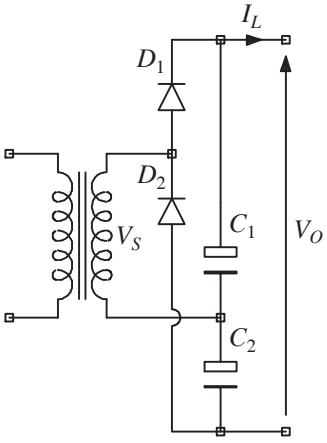

Figure 6