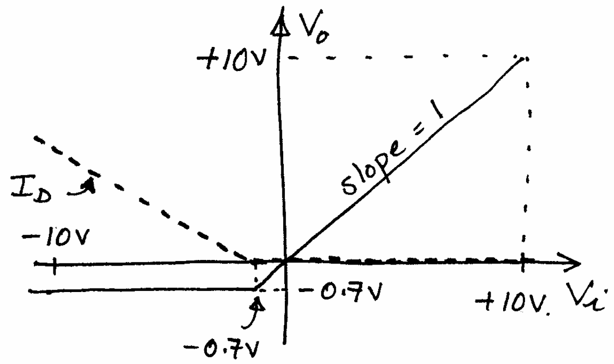
# EEE103 / EEE121 / EEE141 Problem Sheet Solutions

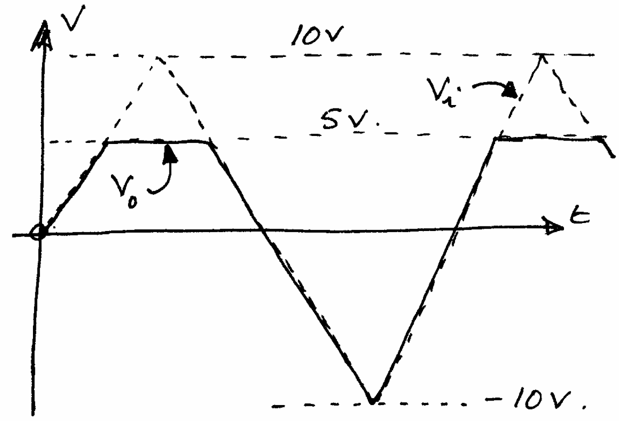
## Diode, Resistor and Capacitor Circuits

Q1 The diode is on the point of conduction when $V_o = -0.7V$. For $V_i < -0.7V$, the diode conducts and $V_o = -0.7$. For $V_i > -0.7V$ the diode does not conduct, no current flows through R so $V_o = V_i$.




$$I_D = \frac{-0.7V - V_i}{R} \text{ for } V_i < -0.7V.$$

Q2 The diode will be on the point of conduction when $V_o = 4.3V + 0.7V = 5V$. For $V_i > 5V$, D will conduct and $V_o$ will be held (by D) at 5V. For $V_i < 5V$, no current flows through R and so $V_o = V_i$.



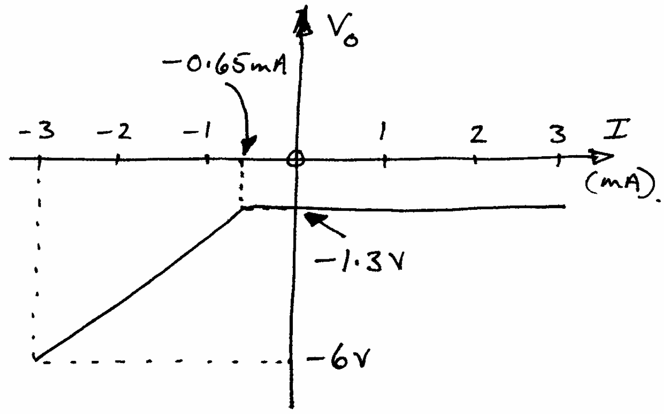

$I_f$ max occurs when the biggest V exists across R — ie, at the positive peak of $V_i$. $I_{f max} = \frac{10V - 5V}{R} = \underline{5mA}$.

Q3 It will be $D_1$ that clips voltages that are too high and $D_2$ that clips voltages that are too low.

For $D_1$ to clip $V_i$ at 3.3V, $V_1 = 3.3V - 0.7V = \underline{2.6V}$.

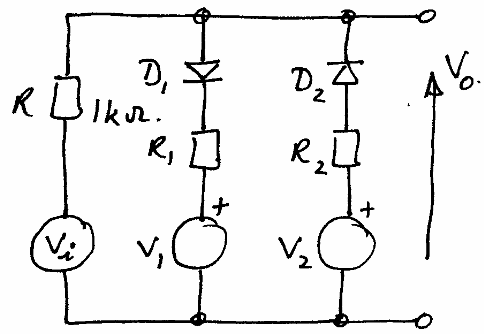
For $D_2$ to clip $V_i$ at 0V, $V_2 = 0 + 0.7V = \underline{0.7V}$.

Q4 The diode will be on the point of conduction if $V_o = -2V + 0.7V = -1.3V$. The value of $I_i$ that will give a $V_o$ of $-1.3V$ with a diode current of zero is $I_i = \frac{-1.3V}{2k\Omega} = -0.65mA$.




For $I_i < -0.65mA$, there is no conduction through the diode so all $I_i$ goes through $R$ and $V_o = I_i R$. For $I_i > -0.65mA$, the diode conducts and $V_o$ is held at $-1.3V$.

Q5 $D_1$ will clip when $V_i > V_1 + 0.7$; $D_2$ will clip when $V_i < V_2 - 0.7$.




To get $D_1$ on point of conduction when $V_o = 3$...

$V_1 + 0.7V = 3$

or $\underline{\underline{V_1 = 2.3V}}$.

To get $D_2$ on point of conduction when $V_o = -5V$,

$V_2 - 0.7V = -5$

or $\underline{\underline{V_2 = -4.3V}}$.

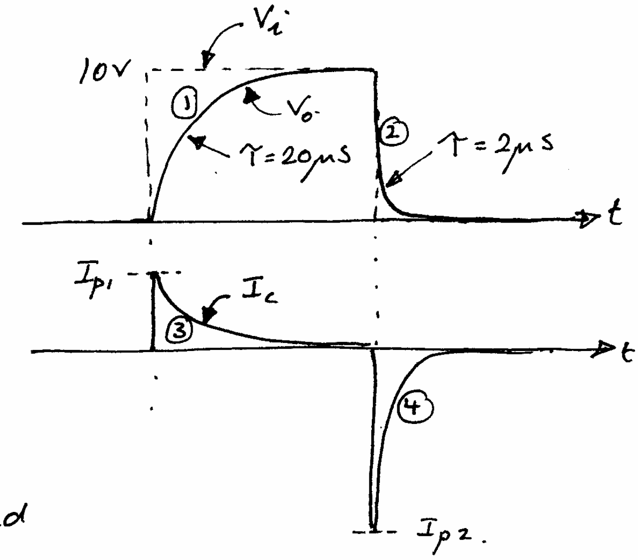
To get a gain of 0.5 for $V_o > 3V$

$$\frac{R_1}{R + R_1} = 0.5 \quad \text{or} \quad \underline{\underline{R_1 = R}} \ (= 1k\Omega).$$

To get a gain of 1/3 for $V_o < -5V$

$$\frac{R_2}{R + R_2} = \frac{1}{3} \quad \text{or} \quad \underline{\underline{R_2 = R/2}} \ (= 500\Omega).$$

Q6 (a) $\tau$ is much shorter than the pulse width so $V_o$ has reached $V_i$ by the end of the pulse.




On rising edge, D is reverse biassed so current flows through $R_2$ to charge C.

On falling edge, D is forward biassed so C discharges through $R_1$ and $R_2$ in parallel.

$I_{p1}$ occurs on leading edge transient....

$$I_{p1} = \frac{V_i}{R_2} = \frac{10V}{2k\Omega} = \underline{\underline{5mA}}.$$

$I_{p2}$ occurs on trailing edge transient....

$$I_{p2} = -\frac{V_i}{R_1 // R_2} = -\frac{10V}{200\Omega} = \underline{\underline{-50mA}}.$$

The four exponential relationships are.

1. $V(t) = 10\left(1 - e^{-t/20\mu s}\right)$.
2. $V(t) = 10\, e^{-t/2\mu s}$
3. $I(t) = 5mA\, e^{-t/20\mu s}$
4. $I(t) = -50mA\, e^{-t/2\mu s}$.

Output pulse width at half height....

$\rightarrow$ time for 1 to reach half height is given by

$$5 = 10\left(1 - e^{-t_1/20\mu s}\right)$$

which leads to $t_1 = 13.86\mu s$.

$\rightarrow$ time for 2 to fall to half height is given by

$$5 = 10\, e^{-t_2/2\mu s}$$

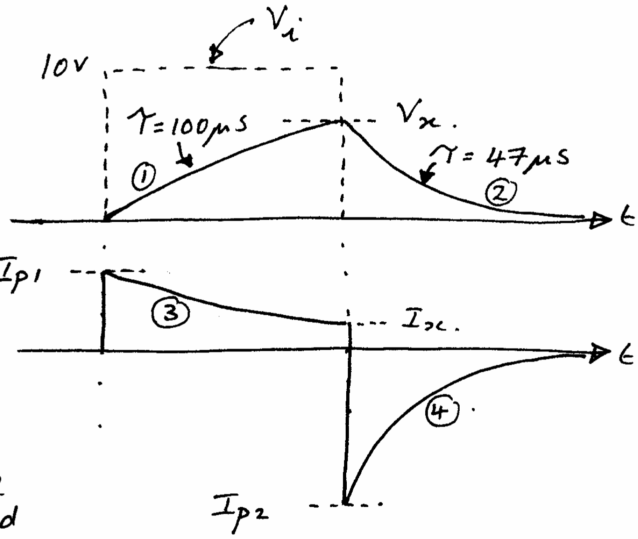
which leads to $t_2 = 1.37\mu s$.

$\therefore$ output pulse width $= 100\mu s - t_1 + t_2$

$= (100 - 13.86 + 1.37)\mu s$

$= \underline{\underline{87.53\mu s}}$

Q6 (b) In this circuit $D_2$ is forward biassed by the leading edge and $D_1$ by the trailing edge. In other words, C charges via $R_2$ and discharges via $R_1$. The charging time constant, $CR_2$ is of the same order as the pulse width so the value of $V_o$ at the end of the pulse, $V_x$, will have to be calculated.




The four exponentials are ....

① $V(t) = 10(1 - e^{-t/100\mu s})$.

② $V(t) = V_x e^{-t/47\mu s}$

③ $I(t) = I_{p1} e^{-t/100\mu s}$

④ $I(t) = I_{p2} e^{-t/47\mu s}$.

We need $V_x$ in order to find $I_{p1}$ and $I_{p2}$, so using ① $V_x = 10\left(1 - e^{-\frac{100\mu s}{100\mu s}}\right) = 6.32V$

$$I_{p1} = {V_i}/{R_2} = \frac{10V}{10k\Omega} = 1mA.$$

$$I_x = \frac{V_i - V_x}{R_2} = \frac{10 - 6.32}{R_2} = 0.368\,mA.$$

$$I_{p2} = -\frac{V_x}{R_1} = -\frac{6.32}{4.7k\Omega} = -1.34\,mA.$$

time for ① to reach 5V given by

$5 = 10(1 - e^{-t_1/100\mu s})$ or $t_1 = 69.3\mu s$.

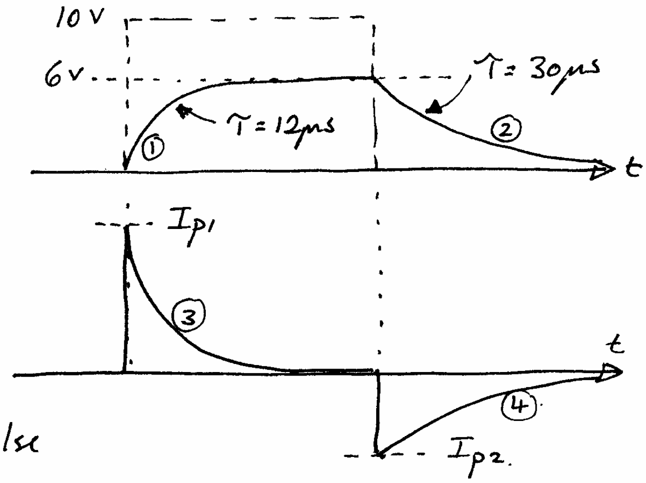
time for ② to fall to 5V given by

$5 = 6.32\, e^{-t_2/47\mu s}$ or $t_2 = 11\mu s$.

output pulse width $= 100\mu s - 69.3\mu s + 11\mu s$

$= \underline{\underline{41.7\mu s}}$.

Q6 (c) In this circuit the diode conducts when $V_i = 10\,V$ but does not conduct for $V_i = 0V$. During the pulse, C charges via $R_1$ but $R_1$ also supplies current through $R_2$ leading to an aiming voltage that is a potentially divided version of the input pulse amplitude.




The four exponentials are

1. $V(t) = 6\left(1 - e^{-t/\tau_1}\right)$ where $\tau_1 = CR_1 \| R_2 = 12\mu s$.
2. $V(t) = 6\,e^{-t/\tau_2}$ where $\tau_2 = CR_2 = 30\mu s$.
3. $I(t) = I_{p1}\,e^{-t/\tau_1}$
4. $I(t) = I_{p2}\,e^{-t/\tau_2}$.

$I_{p1} = \dfrac{V_i}{R_1} = 5mA$. [On the leading edge, $V_o$ is initially zero so all $V_i$ appears across $R_1$.].

$I_{p2} = -\dfrac{6v}{R_2} = -2mA$. [On the trailing edge, D is reverse biased so C discharges through $R_2$]

Half height of $V_o$ is 3V. The time it takes (1) to reach 3V is given by

$$3 = 6\left(1 - e^{-t_1/12\mu s}\right) \quad \text{or} \quad t_1 = 8.3\mu s.$$

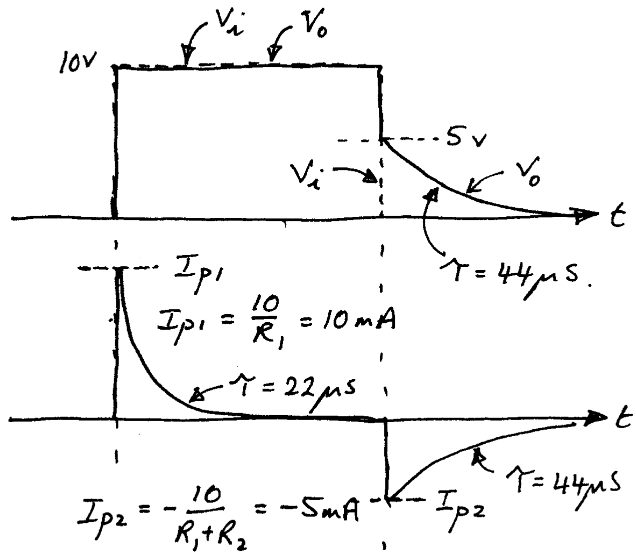
Time taken for $V_o$ to fall to 3V after trailing edge is given by

$$3 = 6\,e^{-t_2/30\mu s} \qquad \text{or} \quad t_2 = 20.8\mu s.$$

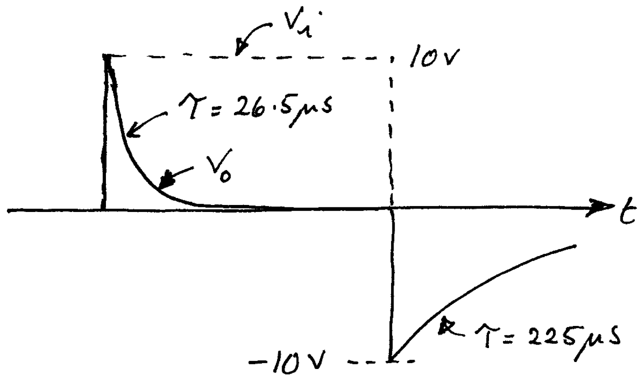
pulse width $= 100\mu s - 8.3\mu s + 20.8\mu s$

$= \underline{\underline{112.5\mu s}}$.

Q7 (i) In this circuit, D conducts throughout the pulse so $V_o = V_i$ for the whole pulse. During the pulse, C charges through $R_1$ so that by the end of the pulse there is ≈ 10V across it. After the trailing edge, D is reverse biassed and C discharges through $R_1 + R_2$ leading to an exponential decay. The output voltage drops abruptly to 5V after the trailing edge because the 10V across C is potentially divided between $R_1$ + $R_2$

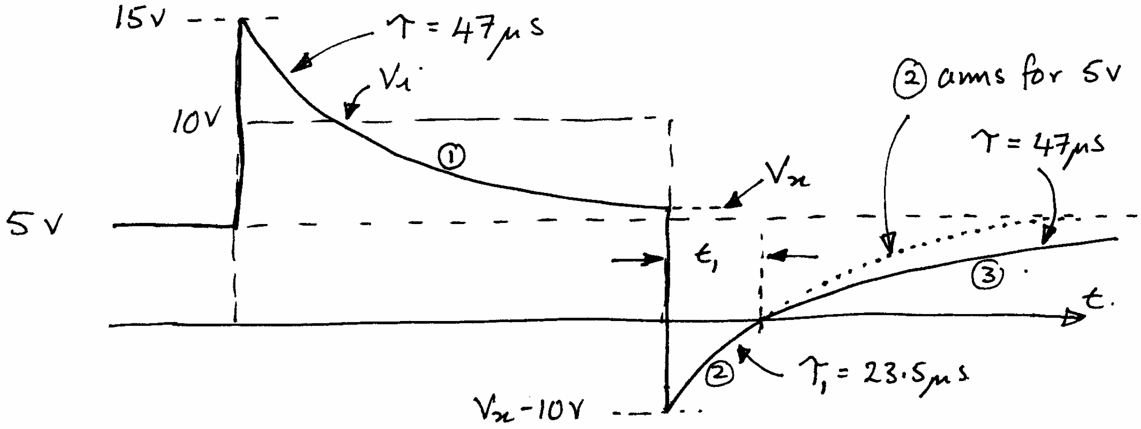



(ii) figure 7b....
Here the leading edge appears at the right hand side of the capacitor making $V_o$ go positive. Hence D conducts and the output voltage approaches zero exponentially with a time constant $CR_1 \| R_2$.




After the trailing edge, $V_o$ is driven to -10V (initially), D is reverse biassed so current flows through $R_1$ only to bring $V_o$ up exponentially towards zero with a time constant of $CR_1$.

figure 7c......
This is the most complicated of the figure 7 circuits. The resting level of $V_o$ before the arrival of the pulse is 5V so the leading edge of the pulse takes $V_o$ instantaneously to 15V. D is then reverse biassed so current flows through $R_1$ making $V_o$ fall exponentially towards 5V with $\tau = CR_1$. $V_o$ will have reached a value $V_x$ by the end of the pulse as shown in the diagram at the top of the next page....




① $V(t) = 10\,e^{-t/\tau} + 5$

② $V(t) = (V_x - 10 - 5)\,e^{-t/\tau_1} + 5$

③ $V(t) = (0 - 5)\,e^{-t/\tau} + 5.$

① gives $V_x$ as 6.19V.

When the trailing edge occurs the output reaches an instantaneous peak of −3.81V and D conducts. D continues to conduct until $V_o = 0$ — ie over $t_1$ — at which point D ceases to conduct and $\tau$ changes from $CR_1 \| R_2$ to $CR_1$. Notice that ② and ③ both aim for +5V but ② starts at −3.81 and is truncated when $V_o = 0$ whilst ③ starts at zero and aims unhindered for 5V.

(iii) To calculate the time between the instant of the trailing edge in figure 7c and the instant at which $V_o$ reaches 2.5V,

use ② to calculate $t_1$ (13.3μs).

use ③ to calculate time to get from 0 to 2.5V (32.6μs).

add the results to give <u>45.9μs</u>.