EEE118: 2012 – 2013 Exam Explanation

J. E. Green

June 1, 2013

This document is an explanation of the exam. It includes the solutions, and how to arrive at them. However, this document is *not* what a student would be expected to produce in an exam situation. The hand written solution document is closer to what *is* expected under exam conditions. This document exists because it is not always clear from hand written exam solutions why some decisions or assumptions were made and where some of the numbers came from. The purpose of this document is to leave no doubt as to why the hand written solutions are correct.

Question 1

This question is about the conduction state of diodes and some common diode circuits.

Part A

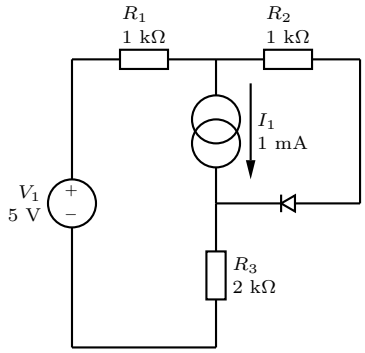

Figure 1: Question 1 part a

Assume Diode is *not* Conducting

- Begin by assuming the diode is not conducting.
- Perform superposition of the voltage source and the current source to find the voltage across the diode terminals.

- The superposition which has the voltage source, V_1, enabled is shown in Fig. 2. The superposition which has the current source, I_1 enabled is shown in Fig. 3.
- In Fig. 2 it can be seen by inspection that no current can flow because there is no continuous conducting pathway.
- Since no current flows there are no $I\,R$ voltage drops across the resistors. The diode has the full 5 V of the voltage source, V_1, across it.

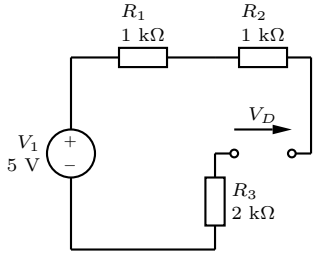

Figure 2: Assuming diode is not conducting. Superposition circuit for the 5 V source, V_1. The 1 mA source, I_1, is open circuit.

- Having established the voltage across the diode due to the 5 V source, V_1, the voltage across the diode terminals due to the current source I_1 must now be determined. The circuit is shown in Fig. 3.
- 1 mA flows through 3 kΩ ($R_1 + R_3$).
- Therefore there is 3 V across the current source terminals.
- R_2 can not drop any voltage because the diode is not conducting ($I_D = 0$), so the diode terminals see the same voltage as appears across the current source.

Note the direction of the voltage across the diode due to the current source, I_1, is *opposite* to the voltage across the diode due to the voltage source, V_1. It may be helpful to redraw Fig. 3 adding some voltage and current arrows if the relationship between V_D due to V_1 and V_D due to I_1 is not apparent.

$$V_D = V_{D\ (5\ \mathrm{V})} + V_{D\ (1\ \mathrm{mA})} \tag{1}$$
$$V_D = 5 + -3 \tag{2}$$
$$V_D = 2\ \mathrm{V} \tag{3}$$

Since $V_D > 0.7$ V the diode is conducting and the circuit must be re-analysed to find the diode current.

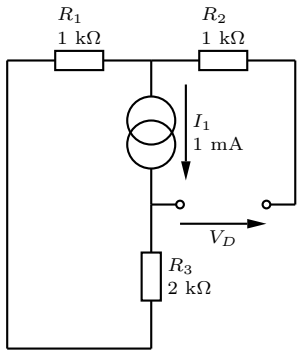

Figure 3: Assuming diode is not conducting. Superposition of the 1 mA source, I_1. 5 V source, V_1, is short circuit.

Diode *is* Conducting

It has been established that the diode is conducting, the question requires that the current flowing in the diode should now be found. Use superposition again but remember that as well as V_1 (the 5 V source) and I_1 (the 1 mA source) the superposition must include the diode which will be replaced with a voltage source, V_D, of magnitude 0.7 V where the more positive terminal is in place of the anode and the more negative terminal is in place of the cathode.

- Superposition begins with the 5 V source, V_1.
- Applying Ohm's law in Fig. 4,

$$I_{D\ (V_1)} = \frac{V}{R} = \frac{5}{4 \times 10^3} = \frac{5}{4}\ \text{mA} \tag{4}$$

The current flowing in the diode due to V_1 (the 5 V source) is 1.25 mA.

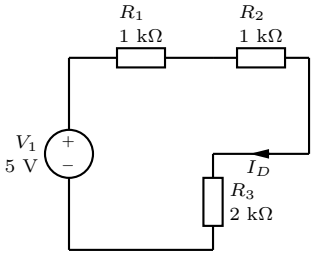

Figure 4: Diode is conducting. Superposition of the 5 V source, V_1. 1 mA source, I_1 is open circuit. Diode is short circuit.

The circuit diagram required to find the diode current flowing due to the 1 mA source is shown in Fig. 5. This circuit can be redrawn as shown in Fig. 6, where it is clearer that the 1 mA leaving the current source will be shared between the

diode pathway (which includes R_2) and the other pathway which is made up of R_1 and R_3. The current will be shared in inverse proportion to the resistances,

$$I_{D\ (I_1)} = -1 \times 10^{-3} \frac{3 \times 10^3}{3 \times 10^3 + 1 \times 10^3} = -\frac{3}{4} \text{ mA} \tag{5}$$

The current in the diode due to I_1 is -0.75 mA.

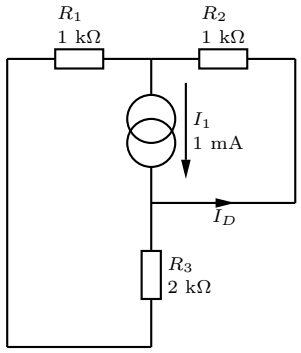

Figure 5: Diode is conducting. Superposition of the 1 mA source, I_1. 5 V source, V_1, is short circuit. Diode is short circuit.

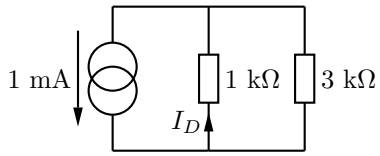

Figure 6: Diode is conducting. Superposition of the 1 mA source, I_1. 5 V source, V_1, is short circuit. This is identical to Fig. 5 but is redrawn for ease of understanding.

All that remains is to find - using superposition - the diode current due to the 0.7 V source that represents the diode in its conducting state. The circuit diagram required to do this is shown in Fig. 7.

- Applying Ohm's law to Fig. 7.

$$I_D = -\frac{V_D}{R_1 + R_2 + R_3} = -\frac{0.7}{4 \times 10^3} = -0.175 \text{ mA} \tag{6}$$

The total diode current is the sum of the three superpositions.

$$I_{D\ (\text{total})} = I_{D\ (V_1)} + I_{D\ (I_1)} + I_{D\ (V_D)} \tag{7}$$

$$= 1.25 \text{ mA} + (-0.75 \text{ mA}) + (-0.175 \text{ mA}) \tag{8}$$

$$= 0.325 \text{ mA} \tag{9}$$

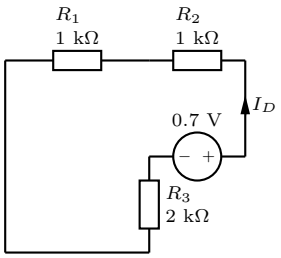

Figure 7: Diode is conducting. Superposition of the diode source, V_D. The 1 mA source, I_1 is open circuit. The 5 V source, V_1, is short circuit. Note the direction of the current flow. It is opposite to the total diode current. The diode is a source of power (energy) in this superposition, consequently its voltage and current must "point" the same way. If they didn't the source would be dissipating power (energy).

Part B

Question 1 Part B asks what current would be required from the source I_1 to put the diode on the edge of conduction. This seems like a lot more work, however the extra calculation is small as two of the results from part A can be used without modification.

- In part A there were three separate calculations to the conduction superposition. I_D due to V_1, I_1 and V_D.
- I_D due to V_1 and V_D has not changed. Only I_1 is now variable.
- The diode current will be 0 A[1] so I_1 will be used to cancel the current caused to flow in the diode by V_1 and V_D
- The current that must be cancelled is therefore,

$$\begin{aligned} I_{D\ (\text{tocancel})} &= I_{D\ (V_1)} + I_{D\ (V_D)} && (10)\\ &= 1.25\ \text{mA} + (-0.175\ \text{mA}) && (11)\\ &= 1.075\ \text{mA} && (12) \end{aligned}$$

- Look again at Fig. 6 which relates the current flowing in the diode pathway to the value of I_1 under the condition that the diode has 0.7 V across it.
- By assessing the ratio of the resistances, three quarters of I_1 flows in the diode pathway (which includes the 1 kΩ resistor).

[1] On the edge of conduction is defined as 0.7 V across anode and cathode, but no current flowing.

- Therefore to cancel a current of 1.075 mA, I_1 will have to be,

$$I_1 = \frac{4}{3}\left(\frac{5}{4} - \frac{0.7}{4}\right) = 1.4\dot{3} \text{ mA} \tag{13}$$

It is wise to substitute this solution into (7) to check that the answer is zero.

An Alternate Method

A student presented the following method on their script this year (June 2013) and obtained full marks for parts A and B of question one. This method is less tedious but requires us to realise that the question can be simplified. R_1 and R_3 can be combined into a single resistor in the position of either R_1 or R_3. Consider that the current flowing in R_1 must be the sum of the current flowing in R_2 and I_1. The same is true for R_3, the diode current (which must also have flowed in R_2) joins with the current in I_1 and both flow through R_3. It is acceptable to move R_3 such that it is in series with R_1 and V_1. This is the situation shown in Fig. 8. From this point it is clear that the two resistors may be summed because they are in series.

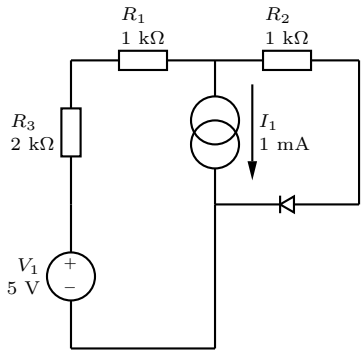

Figure 8: Question 1 part A, alternate method. Rearrangement of the question.

After all simplification the circuit to be analysed is shown in Fig.9. Assume that the diode is not conducting, this reduces the circuit to that shown in Fig.10.

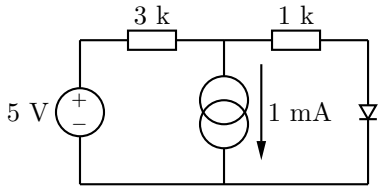

Figure 9: Question 1 part A, alternate method.

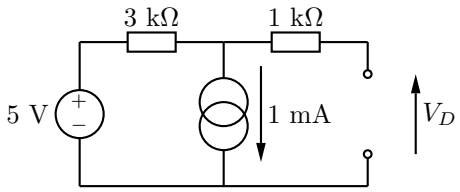

Figure 10: Question 1 part A, alternate method. Diode not conducting.

To decide if the diode is conducting consider the loop including V_1 (5 V), the 3 kΩ resistor and I_1. The other loop, including the diode can not carry any current as the diode is open circuit. The current defined by I_1 (1 mA) flows through 3 kΩ and therefore drops (by Ohm's law) 3 V across it. The 3 V dropped across the resistor is subtracted from V_1 (5 V) to leave 2 V. Since R_2 can not have any current flowing in it, it can not drop any voltage. Hence all of the 2 V appears across the diode. This means our assumption is wrong and the circuit must be re-analysed.

To find the diode current we will use nodal analysis. There is only one unknown node, but there are two unknown loop currents so nodal analysis should require less work than loop analysis. The nodal analysis circuit is shown in Fig. 11.

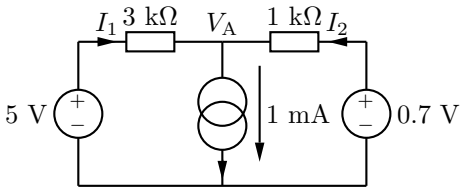

Figure 11: Question 1 part A, alternate method. Nodal analysis to find the current in the diode.

Summing the currents at node A,

$$I_1 + I_2 - 1 \text{ mA} = 0 \tag{14}$$

$$\frac{5 - V_\text{A}}{3 \text{ k}} + \frac{0.7 - V_\text{A}}{1 \text{ k}} - 1 \text{ mA} = 0 \tag{15}$$

after a little transposition we will arrive at,

$$V_\text{A} = \frac{4100}{4000} = 1.025 \text{ V} \tag{16}$$

To find I_D (the diode current) we can find the current in the 1 kΩ resistor, it is in series with the diode so the currents will be the same. Applying Ohm's law to the 1 kΩ resistor,

$$I_D = \frac{0.7 - 1.025}{1 \text{ k}} = -325 \ \mu\text{A} \tag{17}$$

The minus sign tells us that the current flows into the 0.7 V source not out of it as shown in the diagram. This is in agreement with what we know about the circuit - that the diode is represented by the 0.7 V source and therefore must dissipate energy.

Part C

The first part of this question requires the circuit in Fig. 12 to be identified. It is a positive voltage clamp. The input voltage, V_1, is sinusoidal and centred on zero volts. The output voltage, V_o, is taken across R_1 and is a minimum at -0.7 V. When the input voltage tries to fall below -0.7 V the diode conducts and charge moves[1] onto the right plate of C_1 increasing its potential with respect to the left plate. Because R_1 is high valued C_1 discharges slowly through it. Consequently the voltage across the capacitor is unable to fall quickly (current in or out of a capacitor always leads to a change in voltage with time). As V_1 rises the output voltage rises as well but it is greater than the input voltage by whatever voltage the capacitor has charged up to in the prior cycles. This circuit is also called a DC restoration circuit and has uses in voltage multipliers and detection of some types of radio signals.

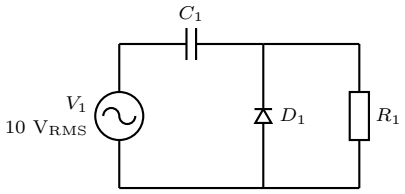

Figure 12: This is the circuit that must be identified in question 1 part c. It is a positive voltage clamp.

The second part of this question asks for a sketch of the current and voltage waveforms for the negative clamp circuit. These can be found in the lecture notes (lecture 5) but are also shown in Fig. 13.

Part D

Part D asks for the voltage multiplier circuit diagram. It is a combination of the clamp and the peak detector and is shown in Fig. 14. The associated graphs are shown in Fig. 15

Note that in these diagrams the diode current is shown but the exam asks for the capacitor current. The difference is that in both the clamp and the peak

[1] we could say "current flows" it is equivalent.

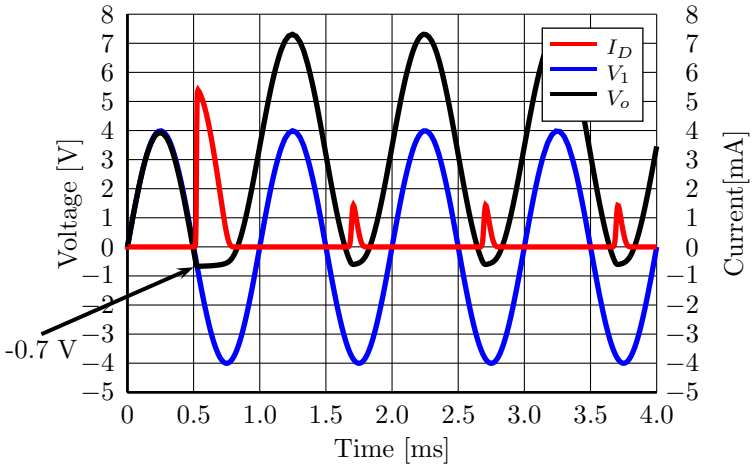

Figure 13: Current and voltage waveforms sketch for the negative clamp circuit

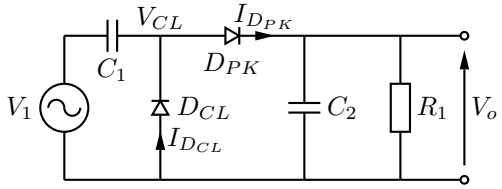

Figure 14: A peak to peak detector circuit.

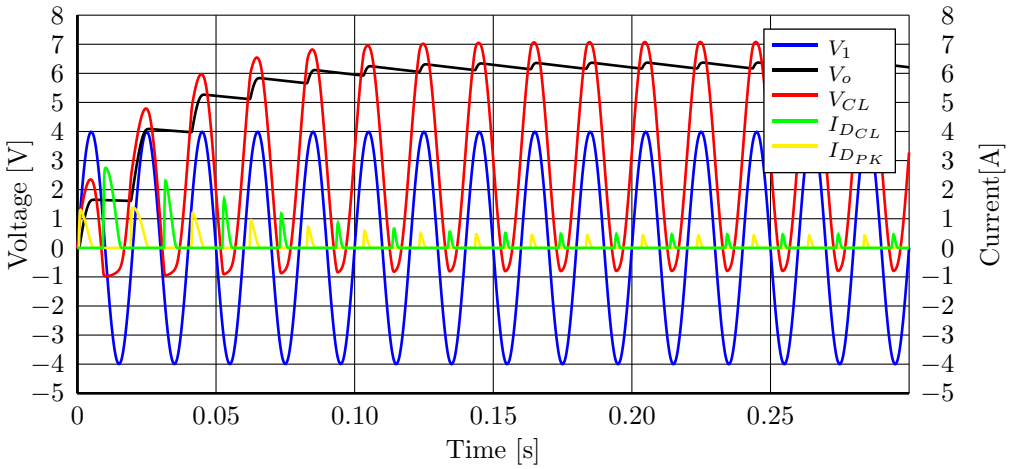

Figure 15: Graphs of current and voltage for the clamp and peak detector sections.

detector parts of the circuit the capacitor discharges slightly when the diode is not conducting. The time constant of note is that the slope on the peak detector output voltage when the diode is not conducting is given by $C_2\,R_1$.

Question 3

This is a question about transistors both in switching circuits and in amplifying circuits.

Part A

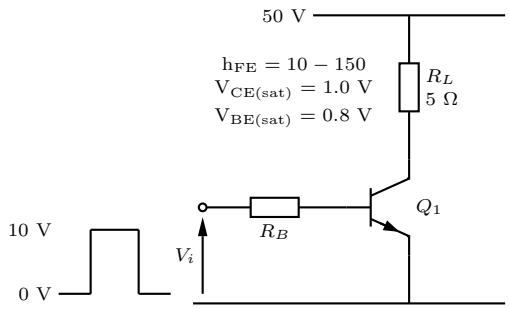

Figure 16: Switching transistor question circuit diagram.

The load current is found by subtracting the collector emitter saturation voltage (1.0 V) from the supply voltage (50 V) to yield the voltage across R_L. Ohm's law is then applied to R_L to find the current flowing in it, this is identical to the collector current.

$$I_C = \frac{V_S - V_{CE(sat)}}{R_L} = \frac{50 - 1}{5} = 9.8 \text{ A} \tag{18}$$

The power in the load can be computed by several methods but here $I^2 R_L$ is used.

$$P_{R_L} = I_C^2 R_L = 9.8^2 \cdot 5 = 480.2 \text{ W} \tag{19}$$

The power dissipated in the switch is given by $V_{CE(sat)} I_C$,

$$P_S = V_{CE(sat)} I_C = 1.0 \cdot 9.8 = 9.8 \text{ W} \tag{20}$$

The range of possible base currents is obtained by looking at the h_{FE} and the collector current (I_C),

$$I_{B(max)} = \frac{I_C}{h_{FE(min)}} = 0.98 \text{ A} \tag{21}$$

$$I_{B(min)} = \frac{I_C}{h_{FE(max)}} = 65.33 \text{ mA} \tag{22}$$

The maximum permissible base resistance is obtained by considering the maximum base current because this yields the smallest value of base resistor. Applying Ohm's law,

$$R_B = \frac{V_i - V_{BE(sat)}}{I_{B(max)}} = \frac{10 - 0.8}{0.98} = 9.38 \ \Omega \tag{23}$$

Part B

Part B concerns the storage of energy in the load. A schematic of the relay model, transistor switch and free-wheeling (D_1) diode are shown in Fig. 17.

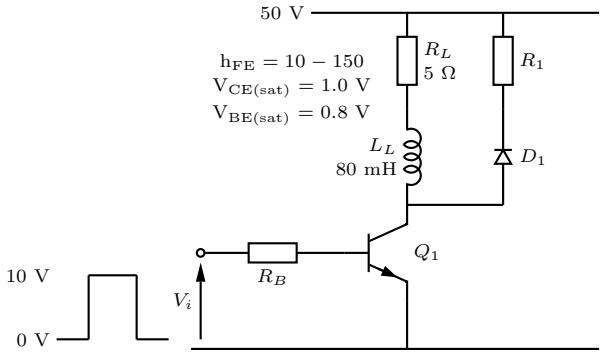

Figure 17: Switching circuit with inductive load and free-wheeling diode. This answers parts i and iv of this question.

The current flowing in the inductor just after the transistor switches off is the same as just before the transistor switches off. This must be the case because the current flowing in the inductor can not change instantly. Similarly the voltage across the plates of a capacitor can not change instantly. R_L has increased from 5 Ω to 15 Ω so the collector current will have reduced, compared to part a, by a factor of three to $3.266\dot{6}$ A.

The energy stored in the inductor is given by

$$E_L = \frac{1}{2} L I^2 = \frac{1}{2} \cdot 80 \times 10^{-3} \cdot 3.266\dot{6}^2 = 0.427 \text{ J} \tag{24}$$

The additions to the diagram required by the last part of this question are shown in Fig. 17. The diode, D_1, provides a conducting pathway when the voltage on the collector rises above the supply rail voltage by more than 0.7 V. This will happen when the relay switches off. The inductor current must continue to flow until the energy stored in the magnetic field around the inductor has dissipated. The energy stored in the magnetic field is converted to a current which is caused to flow by an increase in the voltage across the inductor just sufficient to cause the required current to pass. This sudden increase in voltage on the collector node due to the 'inductive kick' will be enough to destroy the transistor in most cases. To avoid the very high voltage spikes the diode is connected such that it will allow the inductor current to be continuous across the switch off event while clamping the collector voltage to $V_S + 0.7$. The resistor R_1 allows the time constant of the current decay to be set somewhat independently of the load resistance. In the case shown in Fig. 17 the time constant is $\tau = (R_1 + R_L)\, L_L$

Part C

This part of the question is piece of more extended design work in which a transistor set up as an amplifier must have it's design finished. It is necessary to find, R_L, R_E, R_1 and R_2. The conditions of the design are that the output signal should be as large as possible given the constraints of the question. The amplifier circuit is shown in Fig. 18

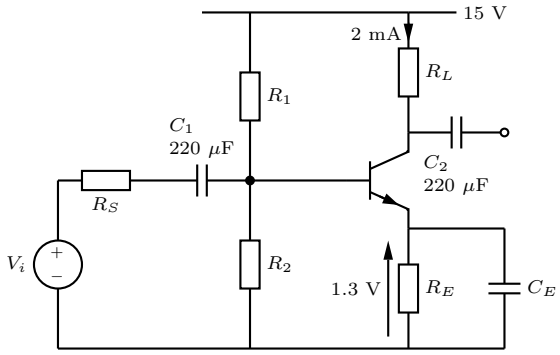

Figure 18: Amplifier circuit for question 2 part d

This question relies on some assumptions on the part of the student. This is done to allow some assessment of the student's ability to make informed decisions to solve problems rather than just to regurgitate mathematics or 'standard answers' from the notes. The question of maximum signal swing is best explained with a diagram (Fig. 19) showing some pertinent voltages in the circuit. The figure caption explains the significance of the diagram. The question sets the emitter voltage at 1.3 V so the base voltage must be at 2.0 V because the base emitter junction of a silicon transistor has approximatively 0.7 V across it when the transistor is in the forward active mode (amplifier). To avoid slipping into saturation mode where both B-E and B-C junction forward biased i.e. transistor behaving like a switch which is "turned on", the collector voltage should not fall below the base voltage by more than 0.7 V. To be safe the base - collector voltage will not be permitted to become any greater than 0 V (remember V_{B-C} is negative in the forward active region). The minimum voltage that the collector can swing to is therefore 2 V. This is where $V_B = V_C$ and $V_{B-C} = 0$. If the collector voltage reaches the supply rail there will be no current in R_L because there will be no voltage across it (Ohm's law) - all of the voltage will be dropped across the transistor, and there will be none left for the resistor hence no current. This represents the condition where the transistor is "switched off". Since the objective is to design a linear amplifier this must not be permitted to happen except at the very highest point of the signal swing. The range of the signal is therefore $15 - 2 = 13$ V, but the mean value of the signal voltage on the collector is $\frac{15+2}{2} = 8.5$ V. This is the quiescent point.

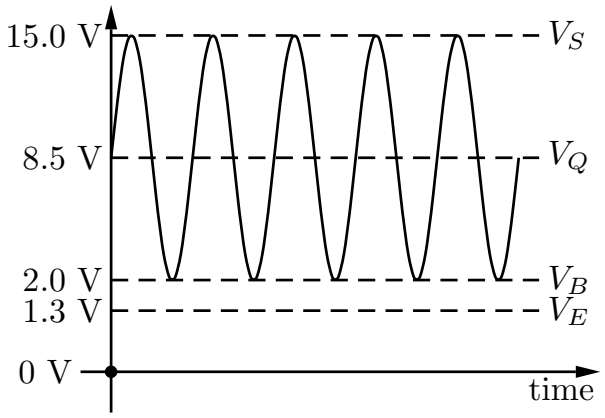

Figure 19: A diagram showing the voltages on the supply, V_S, the collector under quiescent - no signal - conditions, V_Q, the base, V_B, and the Emitter, V_E. The sinusoid represents the maximum signal voltage swing on the collector node from the quiescent point. Notice that the signal is limited by the supply rail on the upper half cycles and by the condition that the collector – base junction should not become forward biased on the lower half cycles. These two limits are reached together, so the quiescent point is half way between them. In terms of maximum signal swing this is an optimal condition.

The tricky part of this question is figuring out the voltage on the collector that allows maximum signal voltage swing. From here on only Ohm's law is required. Several approaches are now possible. R_L will be found first in this solution. The quiescent collector current is given in the question as 2 mA. Now that the quiescent collector voltage is known the value of R_L can be obtained by Ohm's law,

$$R_L = \frac{V_S - V_{C_Q}}{I_{C_Q}} = \frac{15 - 8.5}{2 \times 10^{-3}} = 3.25 \text{ k}\Omega \tag{25}$$

R_1 and R_2 can be worked out together by deciding on a current that flows through them. The decision about this current must be "sensible". That means that the current flowing in R_1 and R_2 should be at least 10 times greater than the base current that will flow into the transistor. If this is done then the base current will represent a maximum of 10 % error in the biasing conditions. The collector current under quiescent conditions will be 2 mA but under full signal swing it will be $\frac{15-2}{3.25 \text{ k}\Omega} = 4$ mA. If $\beta = 100$ is assumed the maximum base current will be 40 μA so 400 μA would be a suitable current to flow in R_1 and R_2. For the sake of simplicity 1 mA will be used. Then $R_1 + R_2 = 15$ kΩ (because there is 15 V dropped across them both and 1 mA flows in them both). We also know that 2 V is dropped across R_2 so it must be 2 kΩ, and therefore $R_1 = 13$ kΩ. The value of R_E is given by assuming negligible base current ($I_C = I_E$) then 1.3 V is across R_E and 2 mA flows through R_E so applying Ohm's law yields, 650 Ω.

Part D

The small signal equivalent circuit for the one transistor amplifier in this question is shown in Fig. 20. The small signal voltage gain is found by first considering the collector - emitter or "output" circuit,

$$v_o = -g_m \ (v_b - v_e) \ R_L \tag{26}$$

Note the minus sign which denotes inversion of the signal. This is consistent with the voltage arrow across the load resistor in the diagram. The current through R_L and voltage across R_L appear to face the same direction. This suggests R_L is delivering energy to the circuit which is not the case. The voltage arrow on the load resistor should have its arrow at the lower end. Consider the input and output voltage arrows assuming that the output arrow was facing the correct (other) way, it should be clear that this small signal equivalent circuit represents an inverting amplifier. The base - emitter or "input" circuit yields,

$$v_b - v_e = v_i \cdot \frac{r_{be}//R_1//R_2}{R_S + r_{be}//R_1//R_2} \tag{27}$$

Substituting the two and solving for v_o/v_i,

$$\frac{v_o}{v_i} = -g_m \, R_L \cdot \frac{r_{be}//R_1//R_2}{R_S + r_{be}//R_1//R_2} \tag{28}$$

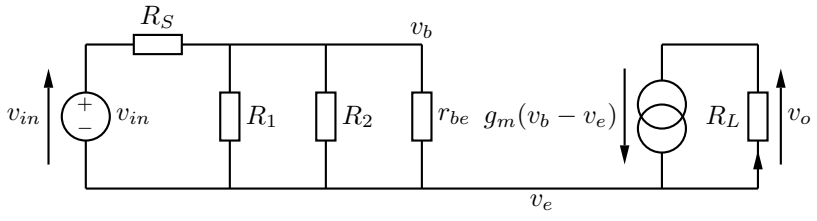

Figure 20: The small signal equivalent circuit of the amplifier in Part C. R_1 and R_2 appear in parallel with r_{be} because the 15 V rail appears connected to ground from the signal's point of view. R_E appears short circuit because it is decoupled by C_E. R_L appears to have one end grounded for the same reason as R_1.

Question 6

This question is about operational amplifiers.

Part A

The symbol for an opamp is shown in Fig. 21.

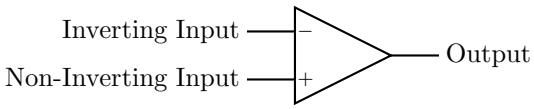

Figure 21: Circuit symbol for an operational amplifier

Typical values for A_o, Z_{in} and Z_{out} are, 10^5 V/V, 1×10^9 Ω and less than 50 Ω.

$$v_o = A_v \cdot \left(v^+ - v^-\right) \tag{29}$$

v_o is the output voltage, v^+ is the voltage on the non-inverting input, v^- is the voltage on the inverting input and A_v is the open loop gain of the opamp.

Part B

The amplifier circuit in Fig. 22 is an inverting amplifier.

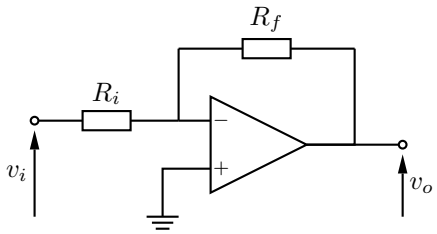

Figure 22: Un-identified opamp circuit in Question 3 part b. It is an inverting amplifier.

The expression for the inverting amplifier gain while assuming that the open loop gain is infinite can be found by summing currents (applying Kirchoff's law for currents in and out of a node) at the inverting input. Summing the current flowing into the node that connects v^-, R_i and R_f,

$$i_f + i_{in} = 0 \tag{30}$$

where i_f is the current flowing in the feedback resistor and i_{in} is the current flowing in the input resistor. There is no current flowing into the v^- terminal of the opamp. This is because the input impedance is assumed infinite - an assumption which follows from the infinite open loop gain assumption.

$$\frac{v_o - v^-}{R_f} + \frac{v_i - v^-}{R_i} = 0 \tag{31}$$

because the open loop gain is infinite the feedback around the opamp will be able to force the inverting and non-inverting inputs to the same voltage. Since v^+ is connected to ground, v^- must also be at ground potential this is known as a "virtual earth".

$$\frac{v_o - 0}{R_f} + \frac{v_i - 0}{R_i} = 0 \tag{32}$$

$$v_o\, R_i + v_i\, R_f = 0 \tag{33}$$

$$v_o\, R_i = -v_i\, R_f \tag{34}$$

$$-v_o\, R_i = v_i\, R_f \tag{35}$$

$$\frac{v_o}{v_i} = \frac{-R_f}{R_i} \tag{36}$$

By a similar method the voltage gain can be found for the situation where the open loop gain is finite. Now v^- and v^+ are not equal. Summing currents at the v^- node,

$$i_f + i_{in} = 0 \tag{37}$$

$$\frac{v_o - v^-}{R_f} + \frac{v_i - v^-}{R_i} = 0 \tag{38}$$

Solve for v^-,

$$\left(v_o - v^-\right)\, R_i + \left(v_i - v^-\right)\, R_f = 0 \tag{39}$$

$$v^- = \frac{v_o\, R_i + v_i\, R_f}{R_i + R_f} \tag{40}$$

Insert (40) into,

$$v_o = A_v \left(v^+ - v^-\right) \tag{41}$$

and remember that $v^+ = 0$, yielding,

$$v_o = A_v \left(0 - \frac{v_o\, R_i + v_i\, R_f}{R_i + R_f}\right) \tag{42}$$

after some intermediary transposition we arrive at,

$$\frac{v_o}{v_i} = \frac{-A_v\, R_f}{R_i + R_f + A_v\, R_i} \tag{43}$$

To obtain the final form divide numerator and denominator by A_v,

$$\frac{v_o}{v_i} = \frac{-R_f}{\frac{1}{A_v}\left[R_i + R_f\right] + R_i} \tag{44}$$

Part C

Part C is a question on the multiple input opamp circuit shown in Fig. 23, the first part of the question asks what value R_4 has to be to give an output voltage of zero. The method is to compute the output voltage due to each source independently and sum them (superposition). In the first part of the question only the DC conditions are required so the input to R_3 reduces to 0.5 V.

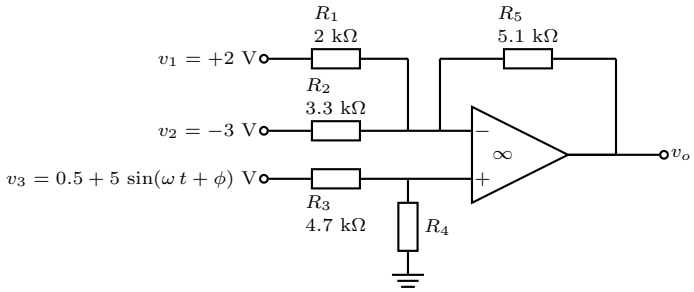

Figure 23: Multiple input opamp circuit.

$$v_o|_{v_3} = \frac{\frac{R_1 R_2}{R_1+R_2} + R5}{\frac{R_1 R_2}{R_1+R_2}} \cdot \frac{R_4}{R_3 + R_4} \cdot 0.5 \tag{45}$$

$$v_o|_{v_2} = \frac{-R_5}{R_2} = \frac{-5.1}{3.3} \cdot -3 = 4.6\dot{3}\dot{6} \text{ V} \tag{46}$$

$$v_o|_{v_1} = \frac{-R_5}{R_1} = \frac{-5.1}{2} \cdot 2 = -5.1 \text{ V} \tag{47}$$

$$0 = v_o|_{v_1} + v_o|_{v_2} + v_o|_{v_3} \tag{48}$$

$$0 = 4.6\dot{3}\dot{6} + (-5.1) + \frac{\frac{R_1 R_2}{R_1+R_2} + R5}{\frac{R_1 R_2}{R_1+R_2}} \cdot \frac{R_4}{R_3 + R_4} \cdot 0.5 \tag{49}$$

Transposing for R_4 and inserting the known resistor values,

$$R_4 = 1.046 \text{ kΩ} \tag{50}$$

Assuming R_4 is 1 kΩ the output due to the AC component of v_3 is given by,

$$v_o = \frac{\frac{R_1 R_2}{R_1+R_2} + R5}{\frac{R_1 R_2}{R_1+R_2}} \cdot \frac{R_4}{R_3 + R_4} \cdot 5 \sin(\omega t + \phi) \tag{51}$$

$$v_o = 4.470 \sin(\omega t + \phi) \text{ V} \tag{52}$$

The phase of the signal is not changed by the amplifier because the signal is input to the non-inverting terminal.