EEE118: Electronic Devices and Circuits

Lecture VI

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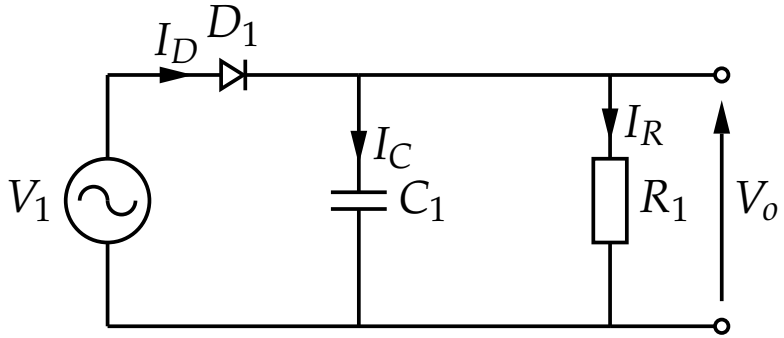
Last Lecture: Review

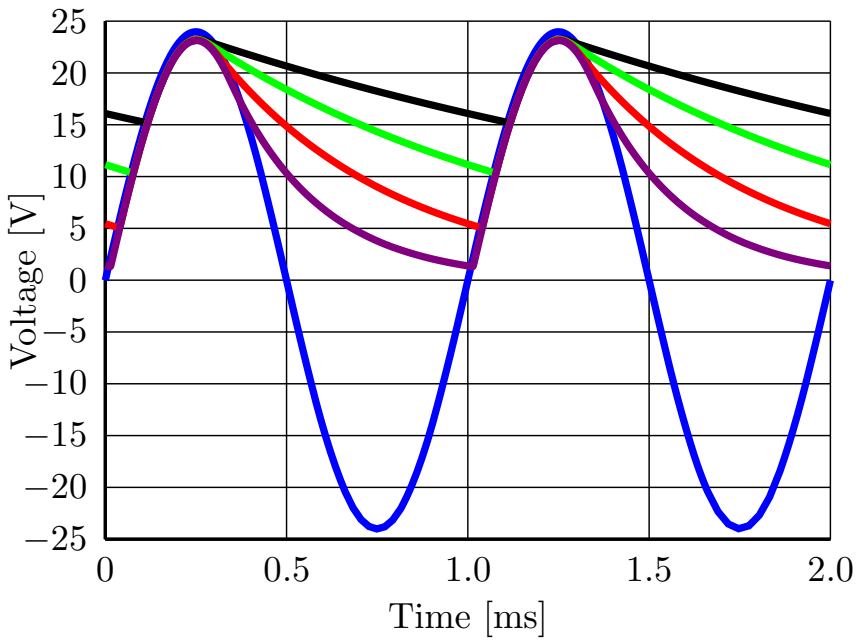
1. Introduced circuits driven by pulses.
2. Noted that, in EEE118 we are concerned with how to treat the circuit operation rather than how to solve differential equations (we will use the solutions without derivation).
3. Developed the idea of a time constant.
4. Looked at a low pass filter driven by a square pulse.
5. Worked through an "exam strength" pulse circuits question.
6. Introduced five diode circuits driven by sinusoids or waveforms derived from sinusoids. These form the basis of discussion from now until after the holidays.
7. Begun a description of operation for the peak detector circuit by thinking about the diode's conduction state as a function of time. A technique we will return to in the future.

Outline

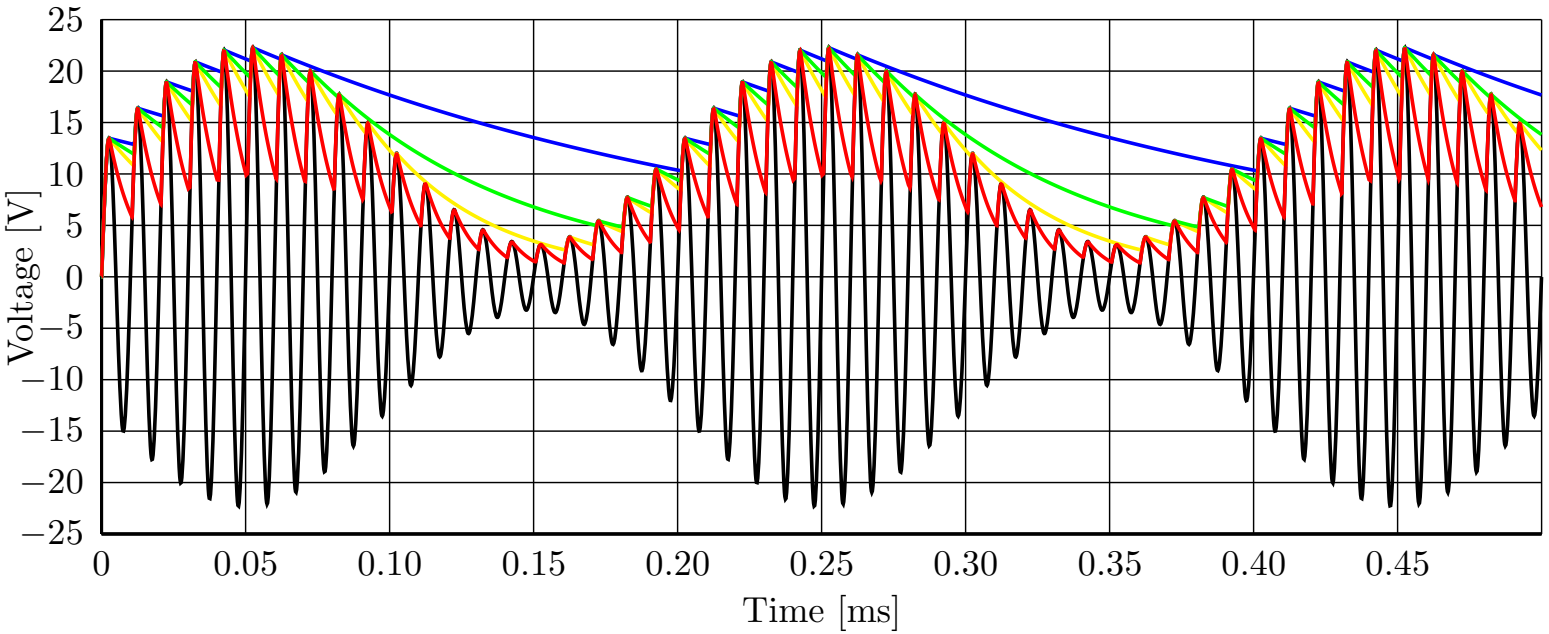
Peak Detector Continued

The time constant $R_1\,C_1$ determines how effective the peak detector is at maintaining the peak signal voltage. It is common to arrange $R_1\,C_1 >> t_p$ where t_p is the period of the waveform. When $t_p = R_1\,C_1$ (green line) the peak detector fails to maintain the peak voltage for the majority of the cycle. As $R_1\,C_1$ is decreased further the exponential nature of the voltage decay becomes apparent and the triangular ripple assumption is broken.





Peak detectors extract information from AM radio signals. RC is a compromise between a value large enough to give a small value of ripple at the carrier frequency and a value small enough to allow the capacitor voltage to follow the modulation envelope.



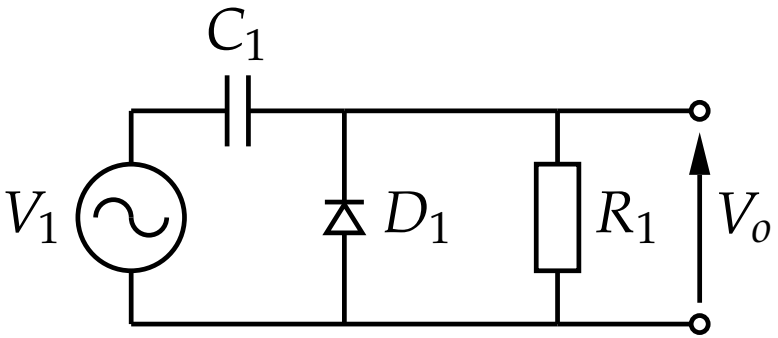
Notice that V_1 (Black), the modulated carrier, has an average value of zero whereas the peak detector output has a non-zero average and a periodicity that is related mainly to the modulation envelope rather than the carrier.

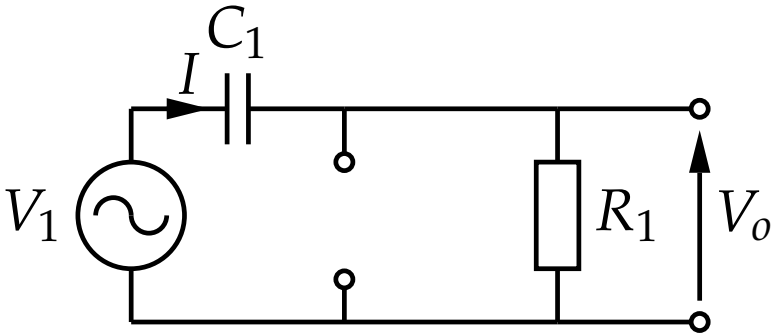
Voltage Clamp

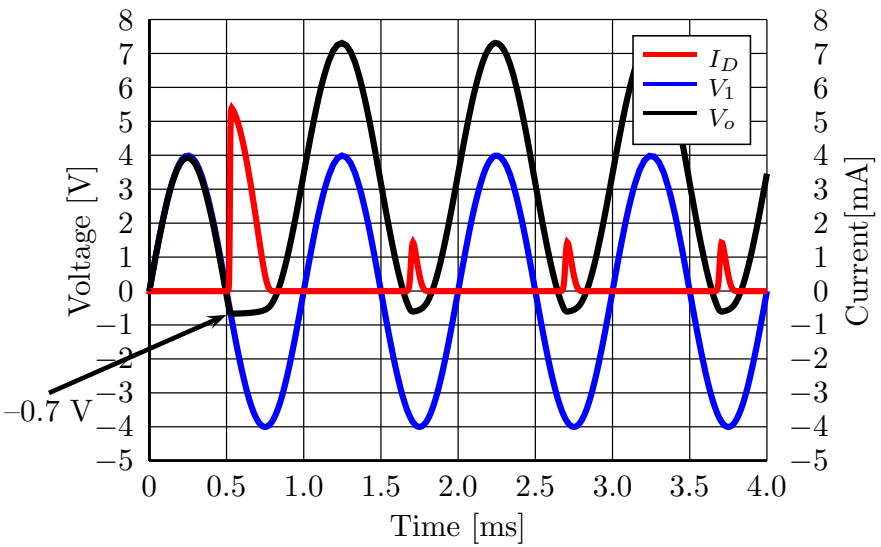
Clamp Description

A circuit that fixes or "clamps" either the positive or negative extreme of a waveform to a defined voltage level.

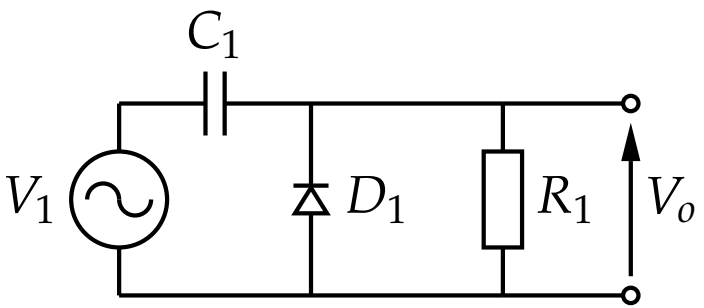
There are some signals that transmit DC level information as part of the signal. The output of a signal detector is simply a waveshape consisting of a DC component and a superimposed signal waveshape. A clamping circuit discards the DC component and defines the DC level of either the positive or the negative signal peaks. Because clamping circuits restores the correct DC levels contained in signals, they are sometimes called "DC restoration circuits" and this term is used frequently in the context of analogue television video signals.

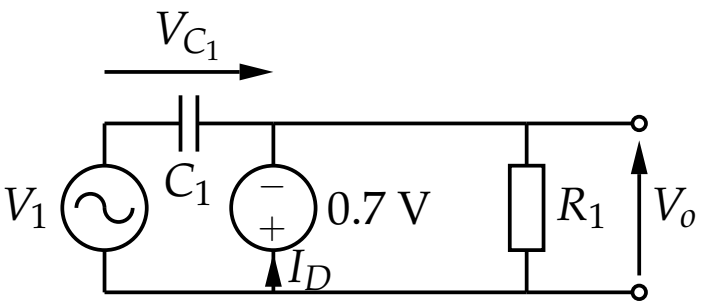


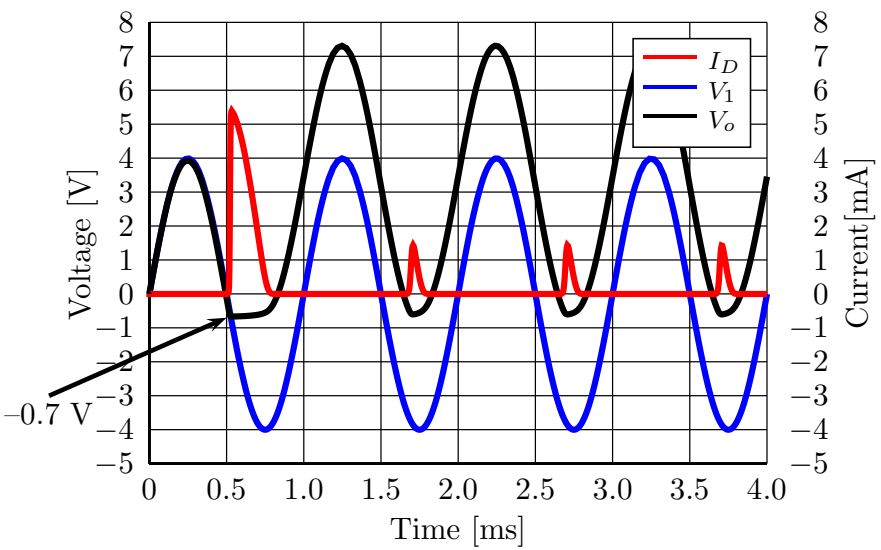




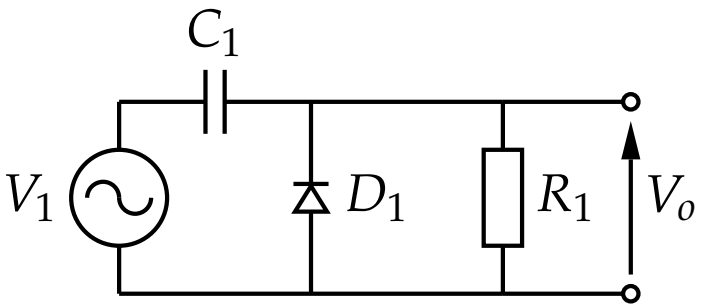
- For the first $^1/_2$ cycle from 0 to 0.5 ms V_1 is positive. The rising V_1 will drive current through C_1 towards the output.
- The diode does not conduct, so current only flows through R_1
- Since R is large, the current flowing does not significantly charge C_1
- There is negligible change of charge in C_1 and so negligible change of voltage across it. So V_o follows V_1

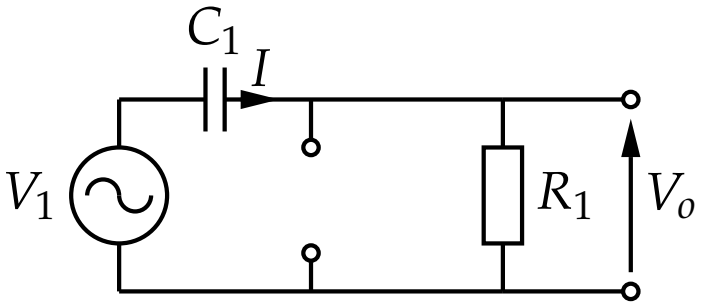


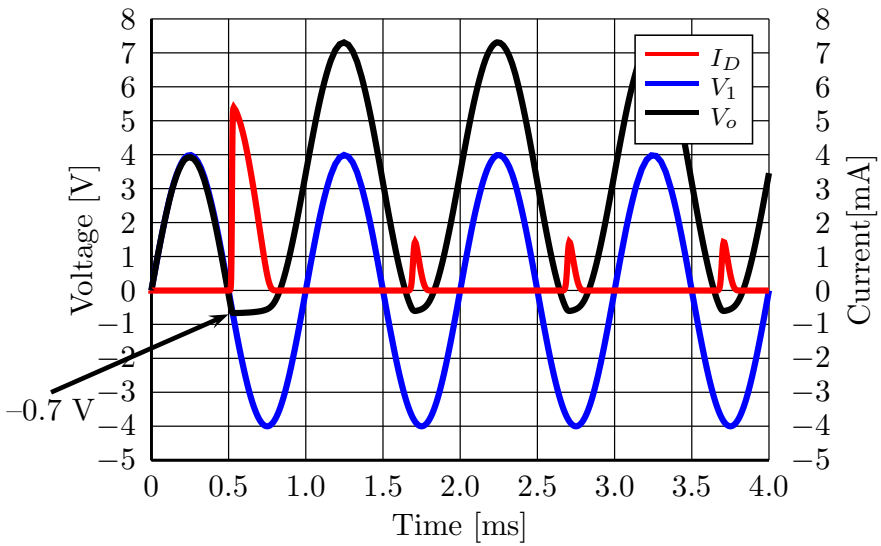




- In the second half cycle V_1 falls and V_o follows until it reaches -0.7 V
- The diode conducts from 0.5 ms - $\sim$ 0.75 ms and holds the voltage at -0.7 V. By the time V_1 has reached its negative peak at 0.75 ms a charge of $C_1 \cdot \left(V_{1_{pk}} - 0.7\right)$ has been stored
- The voltage across C_1 is now $V_{1_{pk}} - 0.7$.

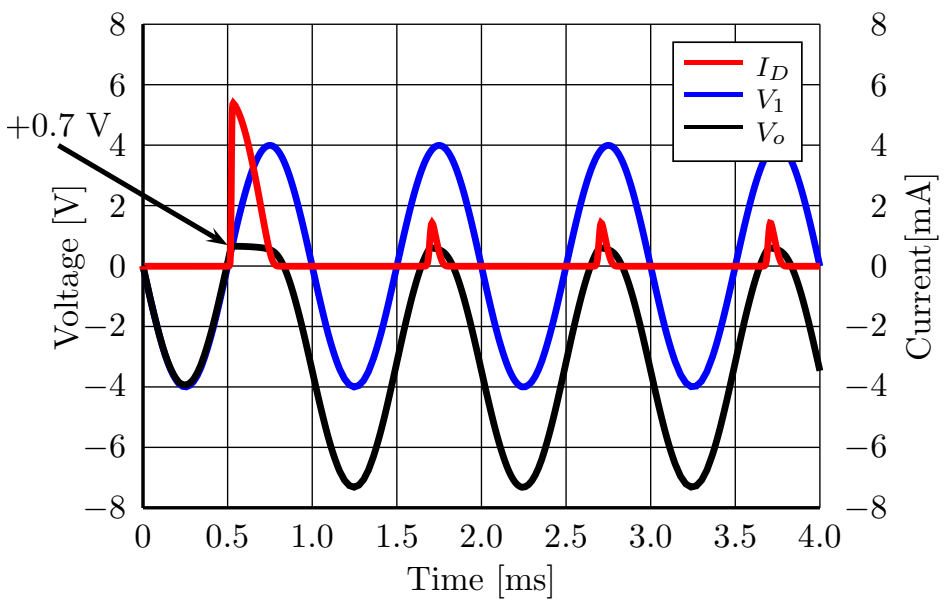






- In the last quarter of the first cycle, V_1 begins to increase again. This rising voltage tries to drive a current through C_1.
- D_1 does not support current flow in this direction. A small discharge current flows from C_1 through R_1 (which is high valued).
- C_1 is not significantly discharged so V_{C_1} remains approximately constant.

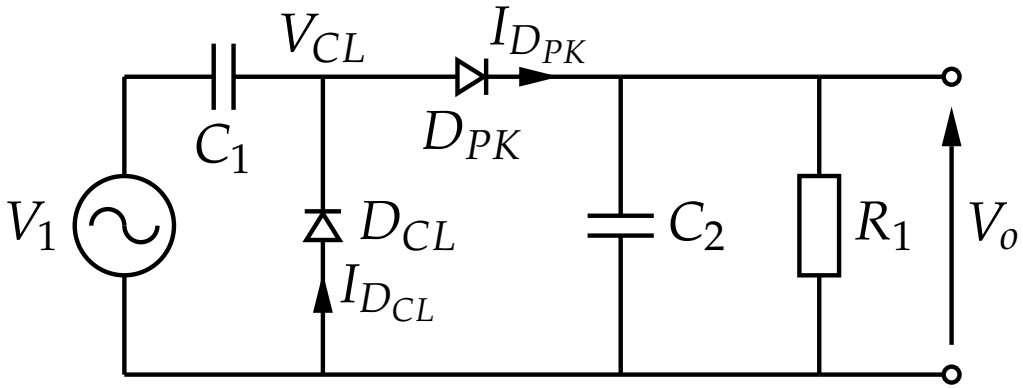
- V_1 could have any additional DC voltage superimposed without affecting the circuit behaviour. The only limit is the voltage rating of the capacitor, C_1
- In practice C_1 must be able to loose charge slowly so that the circuit can follow slowly changing signal amplitudes. R_1 must be finite. But must be sufficiently large to make the charge loss per cycle relatively small
- If the diode is turned around, the positive peaks of V_1 are clamped to +0.7 V and the output goes negative.



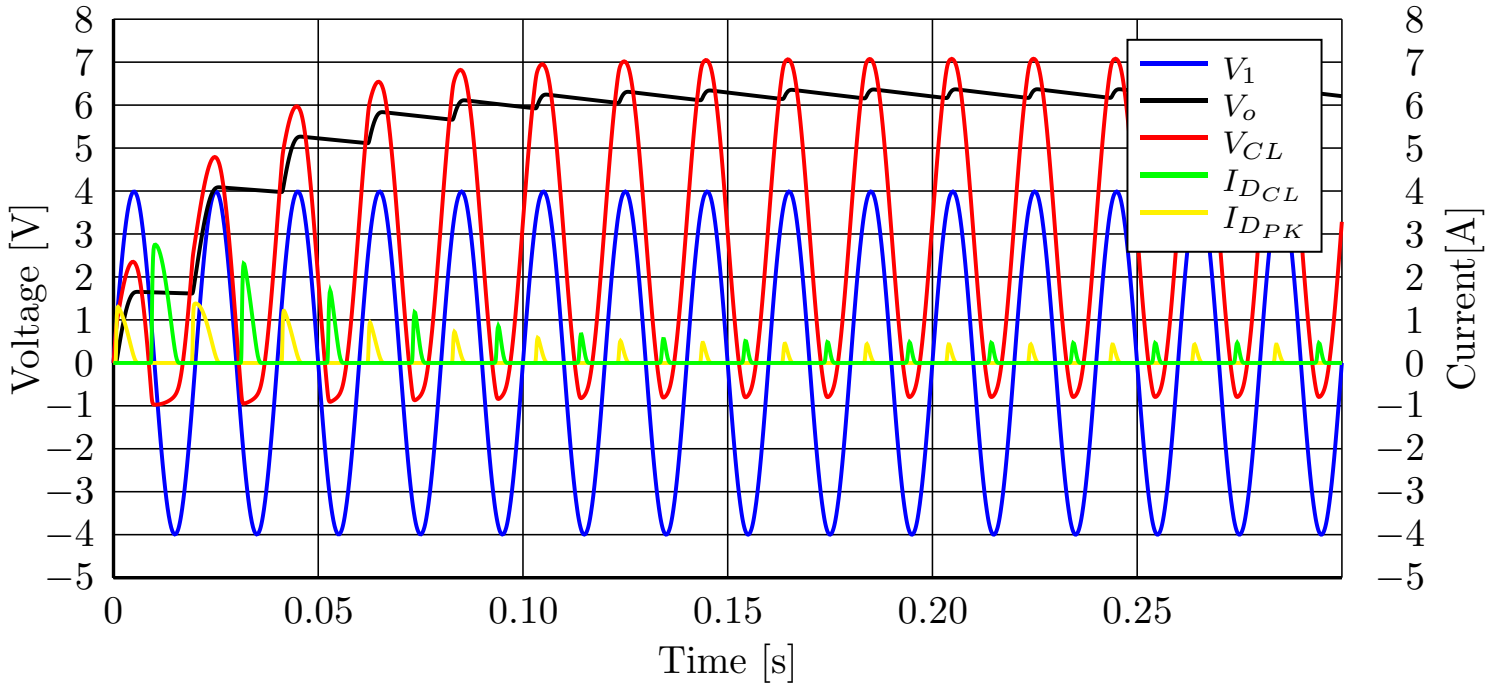
Voltage Doubler

A voltage doubler is a voltage clamp *followed by* a peak detector, also called a peak to peak detector.
The diode clamp takes a sinusoidal signal and clamps the negative peaks to -0.7 V. The peak detector detects the positive peaks to give an output voltage approximately twice what would be expected without the clamp.

C_1 and D_{CL} form the diode clamp and D_{PK} and C_2 form the peak detector. R_1 is the load.



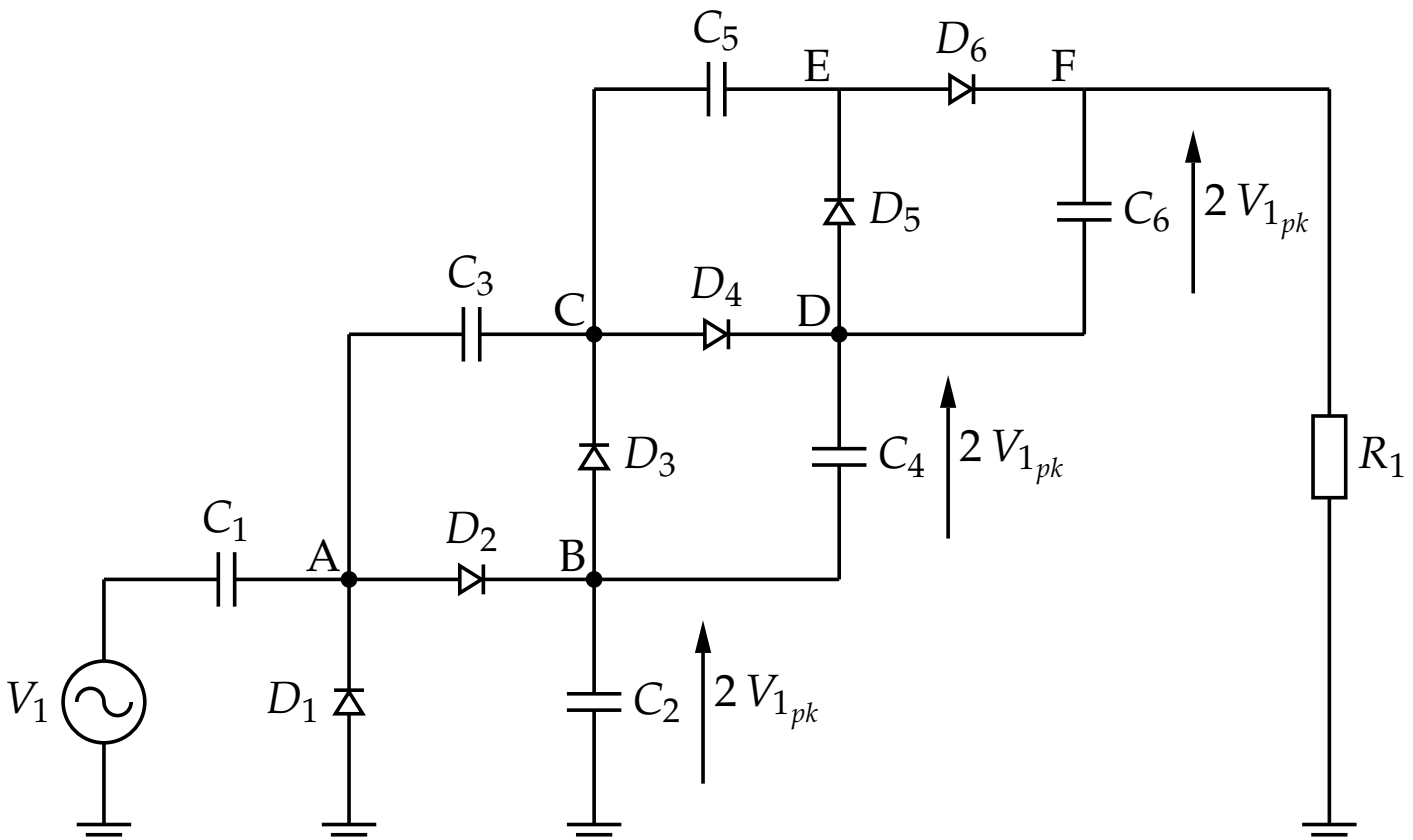
The peak to peak detector is used in signal applications and in low power, power supply applications. The circuit is one of a class of "diode pump" circuits.



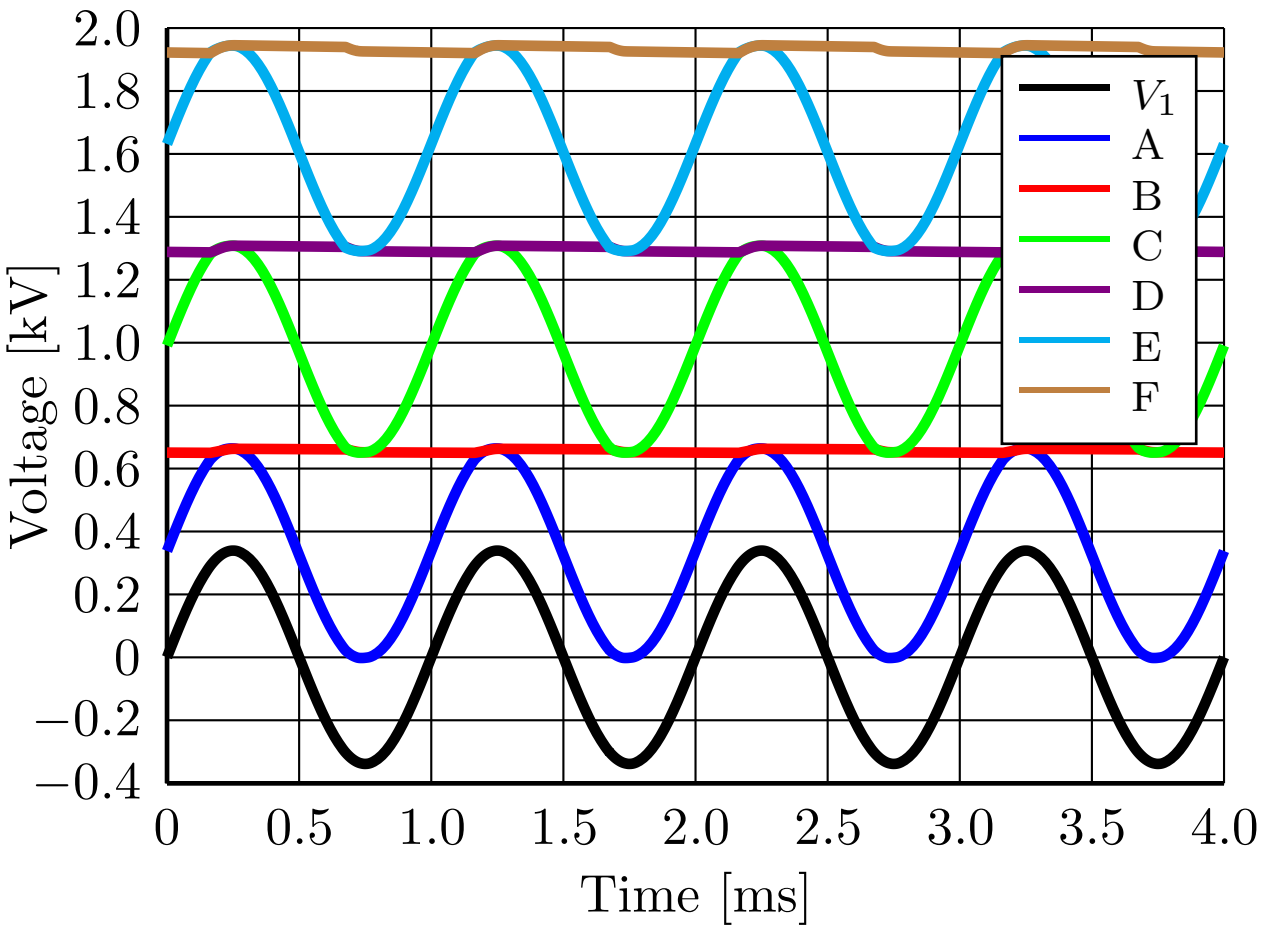
- When V_1 is low, charge flows through D_1 into C_1 as described in the diode clamp explanation.
- When V_1 goes high, that charge is tipped through D_1 into C_2, C_2 is essentially a charge reservoir which is slowly depleted by R_1.
- If C_2 is to be effective, the current in R_1 should yield a small fall in voltage across C_2.

- The output voltage is then determined by the equilibrium condition; charge pumped from C_1 to C_2 per second equals the charge lost through R_1 per second.
- Assuming that C_2 is an effective reservoir, C_1 affects the equilibrium output voltage and the time it takes the output to reach equilibrium.
- If C_1 is small compared to C_2 it will only be able to transfer a small fraction of the charge needed to fill C_2 on each cycle. Charge will build up in C_2 over several input cycles (hence V_o will build up over several cycles) and because the rate at which charge is entering C_2 is small, V_o is sensitive to small current drains such as that through R_1 because of the need to maintain an equilibrium between the charge flowing into and out of C_2 .
- A value of C_1 that is large compared to C_2 can pump a large charge per cycle into C_2 so V_o rises rapidly and is relatively insensitive to current drain through R_1.

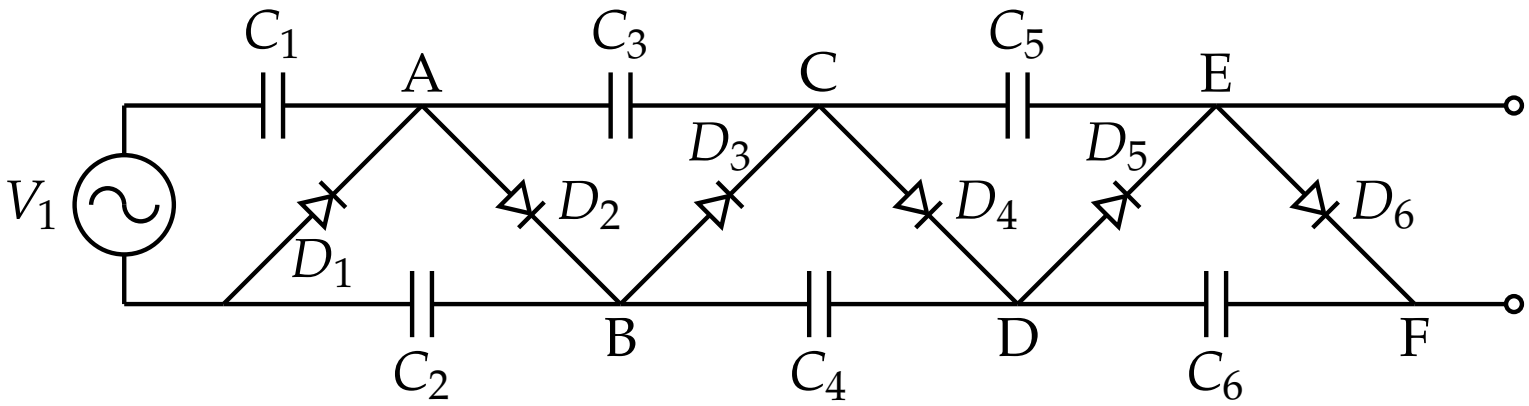
The peak to peak detector circuit can be extended to obtain higher output voltages. C_1, D_1, C_2 & D_2 form a peak to peak detector that generates a voltage across C_2 of $2\,V_{1_{pk}}$. C_3, D_3, C_4 and D_4 form another peak to peak detector. D_3 clamps the negative peak of the signal to a voltage of $2\,V_{1_{pk}}$.



The positive peak of the voltage at B is 2 $V_{1_{pk}}$ above its clamped negative peak (-0.7 V) giving a peak detected voltage across C_4 of 2 $V_{1_{pk}}$. Each peak to peak detector provides an additional 2 $V_{1_{pk}}$. A total of 6 $V_{1_{pk}}$ exists across R_1. $V_{1_{pk}}$ has been multiplied 6 times.



The circuit is normally presented slightly differently.



Applications,

- Cathode ray tube based displays 25 kV. A *flyback converter* (EEE223/EEE307) sometimes used instead
- In integrated form to multiply 5 V pulses up to around 100 V to drive the small plasma displays often found on automotive and 'high-end' CD players
- In experimental physics research to obtain extremely high voltages - of the order of MV - for electric discharge studies. Also electron microscopy

All these applications require low currents - typically a few tens of μA. The circuit is not suitable for high currents.

Homework 2

It should be possible to fully attempt Homework 2 now. It is "due in" 14 days from today.

It should be possible to fully attempt the Diode, Resistor and Capacitor Circuits problem sheet as well.

Review

1. Finished looking at the peak detector circuit.
2. Considered the use of the peak detector in AM radio demodulation
3. Introduced and described the operation of the diode voltage clamp circuit. The clamp can be broken down into,
   - 0° - $\sim 180^\circ$ - Diode not conducting, negligible charging of C through R.
   - 180° - $\sim 270^\circ$ - Diode conducts C charges through D.
   - 270° - $\sim 360^\circ$ - Diode not conducting, small discharge current flows from C through R.
   - All following cycles - Diode briefly conducts around $\sim 270^\circ$ to recharge C
4. Connected a peak detector to a voltage clamp to form a peak to peak detector

Review Continued

- Considered the equilibrium condition that defines how ideally the peak to peak detector acts as a voltage doubler
- Developed a three stage voltage doubler and looked at the voltage on the clamp and peak detector at each stage.
- Observed that the voltage doubler is often drawn as a ladder in which capacitors are the "edges" and diodes are the "rungs"